Interface modification and doping approaches for CdTe thin film solar cells

by **Thomas Shalvey**

Department of Physics

Stephenson Institute for Renewable Energy

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Doctor in Philosophy

January 2021

Abstract

This thesis explores new device structures and processing options for CdTe thin film solar cells by investigating new doping strategies and compositional grading in CdTe, as well as assessing alternative contacts at the front and back interface.

P3HT, spiro-OMeTAD and PFO have been investigated as organic interface layers at the back contact of CdTe solar cells to aid hole extraction. Each device structure was found to have a lower back contact barrier height compared to a device with a simple Au contact, although the inclusion of an organic contact layer increased series resistance and therefore limited peak efficiency. Despite this, an increase in the average device efficiency was observed for all organic contacts due to improved performance uniformity. This is attributed to a pinhole blocking effect whereby the organic layers mitigate shunting losses through areas with weak diode response and is particularly beneficial for devices with thin absorber layers, which are especially susceptible to pinhole formation.

The effect of the addition of sodium to the absorber layer was investigated by incorporating it at different stages during device processing. Evaporation of a thin (~1 nm) NaF layer onto the CdTe back surface prior to metallisation leads to an improved contact and can increase the acceptor density in the bulk, although no significant improvement in device performance was observed. Evaporating NaF prior to the chlorine activation treatment significantly enhances the recrystallization of CdTe in small grained, sputtered material leading to incomplete substrate coverage, but was not observed for large grained films deposited via close spaced sublimation. A combined NaF-$MgCl_2$ treatment of CdS/CdTe devices produced low efficiency devices due to deterioration of the window layer. Replacing the CdS layer with SnO_2 resulting in a more robust device structure which was stable against the aggressive NaF-$MgCl_2$ treatment. The inclusion of NaF in SnO_2/CdTe devices increased the acceptor density by more than an order of magnitude to above $10^{15}cm^{-3}$, and optimal treatment increased peak V_{oc} by 17% compared to a control device without NaF.

The SnO_2/CdTe device architecture was explored further and compared to the standard CdS/CdTe structure. Slow, high temperature CdTe growth conditions increase the average grain size in each case. Interdiffusion of CdS into the absorber layer during CdTe deposition limits the CdS/CdTe structure due to consumption of the window layer. Whilst the SnO_2/CdTe structure prevents such interdiffusion, device efficiency is limited by a weak junction and incomplete substrate coverage due to poor CdTe growth. Depositing onto a SnO_2/CdSe bilayer improves CdTe growth, whilst intermixing during the deposition process encourages the formation of a $CdSe_xTe_{1-x}$ phase which improves the band alignment and long wavelength carrier collection.

Declaration

With the exception of those procedures listed below, all of the work presented in this thesis was carried out by the candidate. No part of this work has been submitted in requirement for any other degree.

- Cross sectional FIB-SEM images presented in Chapter 6 were taken by Leon Bowen, GJ Russel Microscope Facility, Durham University

- ToF-SIMS measurements presented in Chapter 6 were performed by Dr. Sarah Fearn, Department of Materials, Imperial College London

- TRPL measurements presented in Chapter 6 were taken by Dr. Stephen Campbell, Department of Mathematics, Physics and Electrical Engineering, Northumbria University

- XPS measurements presented in Chapter 6 were performed by Huw Shiel, Department of Physics, University of Liverpool

- SEM images of SnO_2/CdTe and SnO_2/$CdSe_xTe_{1-x}$ films presented in Chapter 7 were taken by Dr Heath Bagshaw, Albert Crewe Centre for Electron Microscopy, University of Liverpool

Acknowledgements

I owe an enormous debt of gratitude to everybody who has helped me both scientifically and personally over the past four years, and none more so than to Jon who has consistently offered invaluable guidance and support. His supervision has contributed substantially to my development as a researcher, and to the thoroughly enjoyable experience my PhD has turned out to be. Ken's supervision is also gratefully acknowledged, in particular for his generous scientific help beginning as far back as my undergraduate project, diligent scrutiny of this thesis, and his ever-captivating anecdotes.

I have had the pleasure of sharing an office with Pete, Silvia, Tom, Jack, Huw, Manuel, Luke, Jacob and Matt. I couldn't have asked for a more friendly, helpful bunch to work alongside and spend long days talking, laughing and hearing enough "dad-jokes" to last a lifetime. A great deal of credit to Laurie and Ollie for always being on hand in the lab on the many occasions when things didn't go to plan. Thanks also to Annette, Georgios, Isabel, Kieran and rest of the wider research group who have helped my understanding of various pieces of equipment, measurements techniques and PV in general. Theo, Phil and Nicole deserve specific recognition for patiently listening to my frequent confusion about all things science, and having to repeatedly explain concepts to me.

The SIRE has been a terrific environment in which to spend the past few years. Joe, Tom, Holly, Bruna, Jack, Leanne, Hatem, Olivia, Dan, Alex, and Kieran are thanked for the memorable lunch-time conversations, and a great many more are thanked for the all too frequent coffee breaks, midday football excursions and post-work pints which have offered a welcome distraction from the ordeals of lab work and made the institute a great place to work.

Vince and Matty deserve a special mention for keeping the place together and spending a disproportionate amount of their time helping me 'fix' equipment. The CDT-PV, and in particular Asim, is gratefully acknowledged for funding and support throughout the PhD, as well as C3 who made spending 14 weeks travelling to the different universities to learn about solar cells a great deal of fun. I am also indebted to my friends who have distracted me with golf and beers whenever I'm back in Birmingham, which made writing a thesis sort-of-not-too-bad, and only occasionally reminded me that I spent almost 10 years in university.

I am incredibly lucky to be a part of such an amazing (and enormous!) extended family, to which I owe my thanks. Finally, and perhaps most importantly, I offer my sincere gratitude to my Mom, Dad, Nan, Laura, Joe, Colm, Eamon and Niall, who have been constant sources of support and advice over the past four years and beyond.

Contents

Chapter 1

Introduction

As the global population increases and developing economies continue to improve energy access, primary energy consumption is likely to continue to grow until at least 2050 [1]. Historically, this demand for energy has been met primarily through the burning of fossil fuels, which have enabled rapid economic growth and become central to almost all aspects of daily life. However, this reliance on finite fossil fuel reserves, which have developed over millions of years and are being depleted rapidly, is not sustainable in the long term. Not only does this place ever more pressure on increasingly scarce natural resources, the CO_2 released during fossil fuel combustion is a greenhouse gas which contributes to anthropogenic climate change [2] and therefore poses a more immediate threat. The need for action to limit the environmental damage caused by greenhouse gas emissions has been recognised internationally, leading to the agreement of the Kyoto protocol in 1997 which set legally binding emission reduction targets for the 192 parties involved [3]. The Paris Agreement is the successor to this and was signed in 2015 by 195 nations at the COP-21 meeting, with an aim to limit the global temperature rise to 2°C above pre-industrial levels [4]. To meet these goals, the global energy supply must be rapidly decarbonised and transition towards renewable sources of electricity generation.

Many countries are already undergoing a dramatic shift away from fossil fuel power plants towards renewable sources of electricity generation, most notably wind and solar. This trend is set to continue, even in the most conservative of projections, as shown in Figure 1.1. Solar photovoltaics (PV) in particular has the potential to supply a substantial fraction of the world's energy requirements, and the amount of energy reaching the Earth's surface in the form of sunlight is more than 5,000 times the global yearly demand [5].

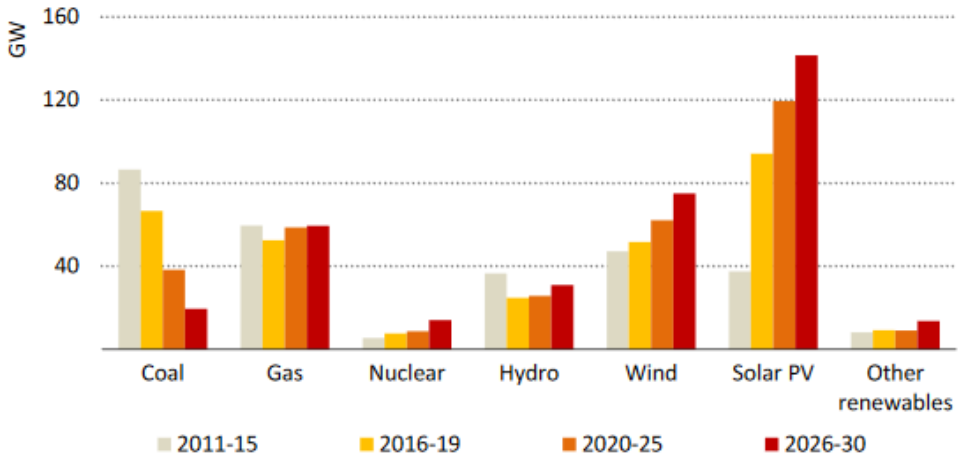

Figure 1.1: Global historical and projected annual power plant capacity additions by technology. Projected capacity additions are based on the WEO "STEPS" stated policy scenario, which assumes only the existing policy announcements already made by governments are implemented. Reproduced from the IEA's "World Energy Outlook 2020" [6]

In recent years, falling cost of solar PV has caused a shift from niche market applications to being the cheapest source of energy in history in favourable locations [6], meaning there is a compelling economic incentive for rapid scale up and deployment. Although numerous types of PV technology exist, the market is currently dominated by crystalline silicon panels. Silicon is an earth abundant semiconductor technology which has benefitted from a mature microelectronics industry, and a record efficiency of 26.7% has been achieved for a single junction monocrystalline cell under standard test conditions [7].

The fabrication of silicon solar panels requires growth of highly pure, large single crystals which are then cut into wafers and assembled into modules [8]. Economies of scale have so far enabled a dramatic cost reduction, allowing this type of manufacturing to be extremely cost efficient [9]. However, to remain competitive and reach lower price per watt, further cost reductions are necessary. Thin film technologies have also been commercialised and currently account for a combined ~5% market share, the majority of which is based on CdTe PV [10]. These technologies offer the prospect of continuous in-line manufacturing of solar panels, which is not possible in the batch-processes required for silicon module production.

The record efficiency of CdTe solar cells is 22.1% [7], which is lower than that of crystalline silicon. However, high deposition rates of relatively impure material directly onto low cost substrates, whilst producing panels of reasonable efficiency, has allowed CdTe modules to provide slightly lower levelized cost of electricity [8]. The standard device architecture has evolved significantly in the past decade, combining a more transparent window layer with a graded absorber layer to increase the short circuit current density close to its theoretical maximum. To further improve device efficiency, the open circuit voltage must also be

increased from 887 mV in the current record device [7] towards its theoretical limit of around 1.1 - 1.2 V [11]. This would require simultaneously increasing hole density whilst improving the bulk minority carrier lifetime of CdTe, as well as reducing the surface recombination velocity at the front and back contacts.

This thesis examines novel architectures for CdTe based solar cells by investigating sodium as a *p*-type dopant, introducing a graded band gap in the absorber layer, and exploring alternative layers at the front and back interfaces. An outline of the structure of this work is given below:

- *Chapter 2* introduces concepts relating to semiconductors and semiconductor junctions relevant to solar cell operation.

- *Chapter 3* provides a review of the development of CdTe based solar cells, including the evolution of device architectures, key processing options and future research directions.

- *Chapter 4* describes several deposition techniques used to deposit layers for CdTe solar cells, as well as the typical experimental conditions used in this work. The working principle of a range of characterisation techniques for thin films and complete solar cells is also provided.

- *Chapter 5* examines three organic compounds as potential back contact layers for CdTe solar cells. Devices with P3HT, spiro-OMeTAD and PFO contact layers were optimised, and compared to a simple Au-only contact. The effectiveness of these organic layers is assessed in terms of device efficiency, back contact barrier height and pinhole-blocking ability.

- *Chapter 6* establishes several routes to incorporating sodium into the CdTe layer by evaporating a layer of NaF onto the back surface. The effect of depositing NaF both before and after chlorine treatment is investigated on different device structures.

- *Chapter 7* evaluates SnO_2 as an alternative window layer to the more commonly used CdS and is combined with a selenium graded absorber layer. A thorough investigation of device processing conditions is given for each device structure.

- *Chapter 8* presents the conclusions from this thesis and suggestions for future work.

1.1 References

1. BP. Energy Outlook 2020 edition. (2020). Available at: https://www.bp.com/en/global/corporate/energy-economics/energy-outlook.html. (Accessed: 3rd December 2020)
2. Intergovernmental Panel on Climate Change. AR5 Synthesis Report: Climate Change 2014. (2014). Available at: http://www.ipcc.ch. (Accessed: 4th December 2020)
3. UNFCCC. Kyoto protocol to the United Nations Framework Convention on Climate Change. (1998). Available at: unfccc.int/kyoto_protocol. (Accessed: 4th December 2020)
4. UNFCCC. Adoption of the Paris Agreement. (2015). Available at: unfccc.int/process-and-meetings/the-paris-agreement/the-paris-agreement. (Accessed: 4th December 2020)
5. Tress, W. *Organic Solar Cells*. **208**, (Springer International Publishing, 2014).
6. International Energy Agency. World Energy Outlook 2020. (2020). Available at: https://www.iea.org/reports/world-energy-outlook-2020. (Accessed: 3rd December 2020)
7. Green, M. A. *et al.* Solar cell efficiency tables (version 56). *Prog. Photovoltaics Res. Appl.* **28**, 629–638 (2020).
8. Wilson, G. M. *et al.* The 2020 photovoltaic technologies roadmap. *J. Phys. D. Appl. Phys.* **53**, (2020).
9. Fraunhofer ISE. Levelized Cost of Electricity - Renewable Energy Technologies. (2018). Available at: https://www.ise.fraunhofer.de/en/publications/studies/cost-of-electricity.html. (Accessed: 4th December 2020)
10. Fraunhofer ISE. Photovoltaics Report. (2020). Available at: https://www.ise.fraunhofer.de/en/publications/studies/photovoltaics-report.html. (Accessed: 4th December 2020)
11. Geisthardt, R. M., Topič, M. & Sites, J. R. Status and potential of CdTe solar-cell efficiency. *IEEE J. Photovoltaics* **5**, 1217–1221 (2015).

Chapter 2

Physics of photovoltaic devices

2.1 Introduction

The photogalvanic effect, whereby a voltage is induced across a system in response to light exposure, was first reported by Becquerel in 1839 in an electrolytic cell [1]. The first solid state system to demonstrate the photovoltaic effect was based on a selenium Schottky junction with gold [2], although a practical solar cell based on a silicon *p-n* junction was not developed until 1954 [3]. This chapter reviews the underlying physics describing the operation of these photovoltaic devices whereby electron-hole pairs are photogenerated and separated to output electricity. General design rules for efficient solar cell development are discussed.

2.2 Properties of Semiconductors

2.2.1 Band structure of crystalline materials

Modern solar cells are based on crystalline semiconductors whereby atoms are arranged periodically in a repeating unit cell. The electrons associated with each isolated atom occupy discrete energy levels, which are split when brought into close proximity to other atoms in order to fulfil the Pauli exclusion principle. For a many atom system, the repeated splitting of closely spaced energy levels gives rise to near-continuous energy bands and in the case of crystalline materials this results in a band structure consisting of allowed and non-allowed energy bands. The occupations of these bands are described by Fermi-Dirac statistics, and at absolute zero all electrons occupy the lowest available energy state.

Metals have band structures such that the outermost energy band is partially filled and therefore electrons can move freely throughout the material, resulting in high conductivity. Non-metals are characterised by a band gap (E_g) in which there are no available energy states between the outermost filled energy band (valence band - E_V) and the next highest band (conduction band – E_C), which is empty at 0 K. Semiconductors have a band gap that is small enough for electrons to be thermally excited from the valence band into the conduction band at room temperature thereby creating free carriers, whereas insulators have larger band gaps across which thermal excitation is negligible.

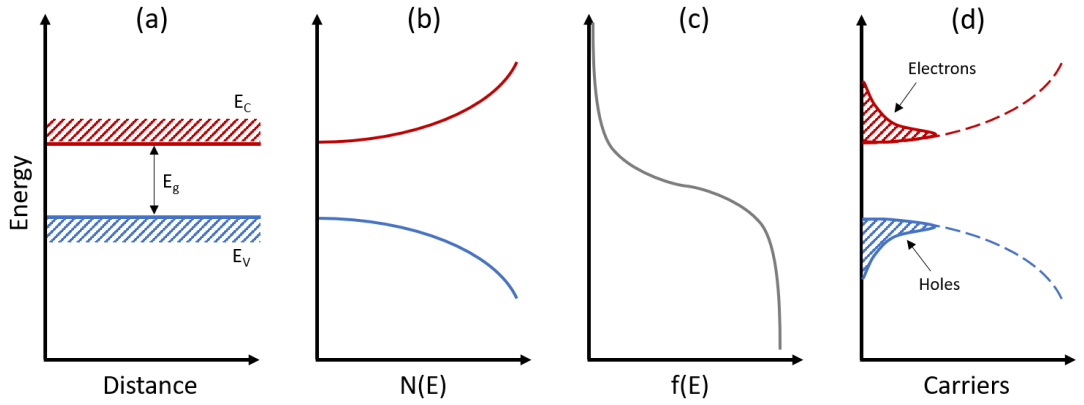

Figure 2.1: (a) schematic band diagram showing conduction and valence bands with corresponding band gap, (b) density of states in each band, (c) probability of occupation at T > 0 K and (d) the resulting distribution of electrons and holes in the valence and conduction bands

Figure 2.1 demonstrates how the band structure of a semiconductor allows for free carriers in both the valence and conduction band at temperatures above absolute zero [4]. The density of states within a semiconductor ($N(E)$) is zero inside the band gap and increases rapidly away from the band edges. The probability of occupation of these states is described by the Fermi distribution ($f(E)$), which implies that above absolute zero, some electrons will be thermally excited across the band gap to occupy states within the conduction band leaving behind empty states (holes) in the valence band. This results in an intrinsic carrier concentration (n_i) of free charge carriers in the valence and conduction bands at a given temperature for a semiconductor in thermal equilibrium.

2.2.2 Light absorption and direct/indirect transitions

When a semiconductor is illuminated, the absorption of a photon with sufficient energy ($h\nu > E_g$) can allow carriers to be excited across the band gap, whereas lower energy photons are transmitted without excitation. Since both energy and momentum must be conserved upon the absorption of a photon, semiconductors with a direct fundamental band gap shown in Figure 2.2a (where the conduction band minimum and valence band maximum have the same *k*-vector) tend to have high absorption coefficients of above band gap radiation. Indirect semiconductors require a two-step absorption process involving both a photon and phonon to excite carriers across the band gap as shown in Figure 2.2b. This process is much less likely to occur and therefore indirect band gap semiconductors tend to have lower absorption coefficients. As a result, direct band gap absorbers can typically absorb most of the solar spectrum within the first < 5 μm, whereas indirect absorbers need to be an order of magnitude thicker to absorb a similar fraction.

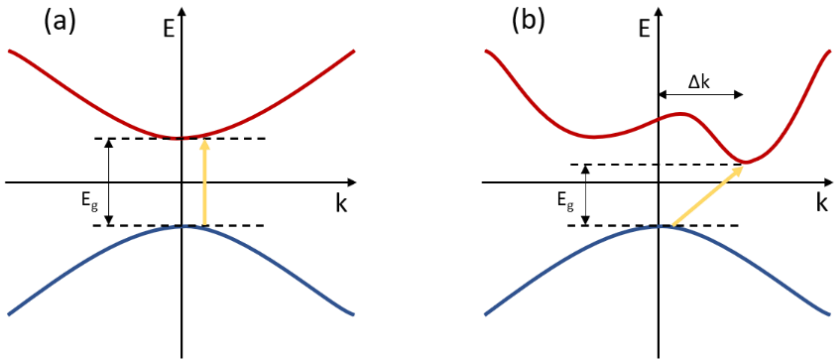

Figure 2.2: Energy – momentum diagrams showing examples of semiconductors with (a) direct and (b) indirect fundamental band gaps and the electronic transitions accompanying photon absorption

Once an electron – hole pair is generated by the absorption of a photon, this excited state will tend to revert to its lower energy state through recombination after an average time τ. If an electron in the conduction band transitions directly into to the valence band, a photon of energy equivalent to the band gap is emitted and the recombination occurs radiatively. As with absorption, the emission of a photon from an indirect band gap semiconductor also requires emission of a phonon to conserve momentum. This decreases the likelihood of radiative recombination, meaning indirect semiconductors tend to have longer radiative carrier lifetimes than direct band gap semiconductors.

A density of states within the band gap can aid recombination whereby a hole from the valence band and electron from the conduction band simultaneously relax to the defect level in a two-step process and recombine. In this case no photon is emitted, and the recombination occurs non-radiatively. This is explored further in section 2.5.3.

2.2.3 Semiconductor doping

For intrinsic semiconductors with similar density of states in the conduction and valence band, the number of carriers in each band is the same and therefore the Fermi level is located near the middle of the band gap. The addition of impurities into a semiconductor introduces localised energy levels and therefore leads to a density of states within the band gap. Impurity levels that are close to either band edge are likely to be ionised at room temperature, which therefore increases the free carrier concentration within the nearby energy band. The introduction of donor atoms with energy level (E_D) close to the conduction band minimum (CBM) results in *n*-type doping and shifts the Fermi level closer to the conduction band. Likewise, ionised acceptor states (E_A) close to the valence band maximum (VBM) result in *p*-type doping and lower the Fermi level towards the valence band, as shown in Figure 2.3.

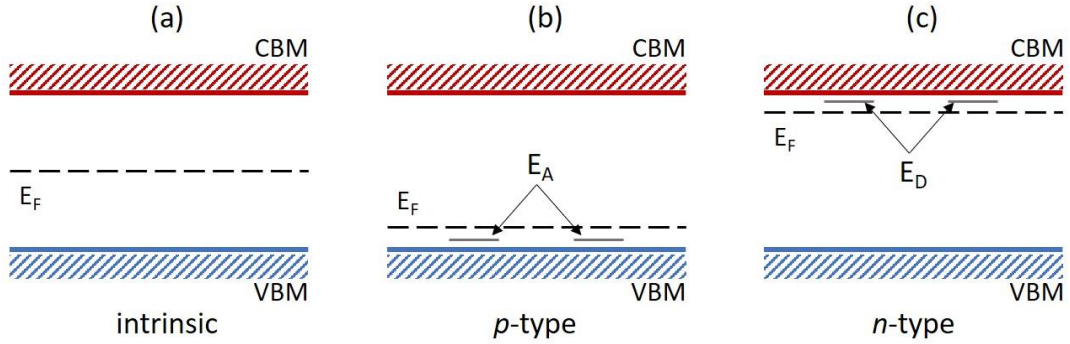

Figure 2.3: Diagram showing the position of the Fermi level (E_F) relative to the valence band maximum and conduction band minimum for (a) intrinsic, (b) *p*-type and (c) *n*-type semiconductors, as well as the location of acceptor (E_A) and donor (E_D) energy levels which increase the carrier concentration in the valence and conduction bands respectively when ionised.

2.3 Semiconductor junctions

The use of a suitably chosen semiconducting material will allow photons to be absorbed and therefore electron – hole pairs to be generated. By design of an appropriate junction, which creates an internal electric field, the carriers are then collected at selective contacts to an external circuit before they have a chance to recombine. This electric field is created by the requirement for a continuous Fermi level across a semiconductor-metal, or semiconductor-semiconductor, interface whereby a difference in chemical potential causes electrons and holes either side of the junction to diffuse across the interface and recombine. This leaves behind fixed ionic charge in both materials that prevents further electron flow thereby establishing an equilibrium at the interface, with a built-in electric field and region substantially depleted of free charge carriers. The main junction types relevant to photovoltaic applications are *p*-*n* homojunctions and heterojunctions as well as Schottky junctions, with a brief description of each given below and described more fully in refs [5,6].

2.3.1 Homojunctions

A homojunction is formed when *n*-type and *p*-type doped variants of the same semiconductors are brought into contact with each other, with the resulting alignment of Fermi levels forming a *p*-*n* junction shown in Figure 2.4. Fermi level alignment requires that the work function of the *n*-type (ϕ_n) and *p*-type (ϕ_p) semiconductors be equal. To accommodate this, and to maintain a continuous electron affinity (χ) and band gap (E_g) on either side of the junction, the vacuum level (E_{vac}), valence band (E_V) and conduction band (E_C) vary with respect to the Fermi level as a function of position. This band bending creates a built-in voltage (V_{bi}) across the interface which is equal to the difference in work function of the two doped regions and defines the maximum voltage that could be extracted from the junction.

Since the two layers consist of the same semiconductor material with the same band gap, there are no discontinuities in the band diagram and therefore no impediments to carrier flow across the junction caused by band offsets. Silicon solar cells utilize homojunctions by diffusion of extrinsic dopants from a surface to overcome the existing doping. However, this approach is less feasible for direct band gap absorbers since carriers are generated much closer to the surface than for indirect band gap absorber where recombination is more likely and therefore heterojunctions are typically used instead.

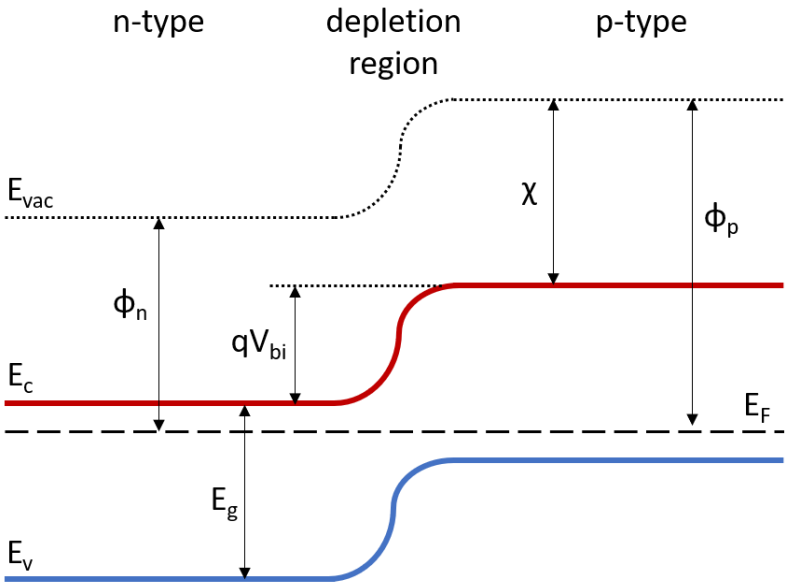

Figure 2.4: Example of a homojunction band diagram formed between *p*-type and *n*-type layers of the same semiconductor under short circuit conditions.

2.3.2 Heterojunctions

Heterojunctions are formed by an interface between two distinct semiconductors with different Fermi levels. As with homojunctions, band bending is induced by the alignment of Fermi levels which establishes a built-in potential across the interface. Since the two materials may have different band gaps and electron affinity, discontinuities in the band structure can arise as described by the Anderson model [7]. Figure 2.5 shows an example of a heterojunction where the *n*-type layer has a larger band gap and smaller electron affinity than the *p*-type layer, which results in offsets in the conduction band and valence band at the junction interface. These discontinuities can act as barriers to carrier transport across the junction and their presence is an important consideration when designing a heterojunction.

The use of two different semiconductors for each side of the junction allows for more flexibility in solar cell design, and typically results in the use of a large band gap, *n*-type 'window' layer contacted to a highly absorbing *p*-type layer with a smaller band gap. This ensures that photons are absorbed in, or near to, the depletion region where the electric field is largest and can therefore aid carrier separation. Heterojunctions may have a high density of interfacial defect states due to the use of dissimilar materials with potentially different crystal structure and lattice constants. To compensate for this, and avoid excessive interface recombination, the window layer is typically more highly doped to ensure the electric field resides primarily in the absorber layer. The band bending then occurs predominantly within the absorber which results in type inversion at the interface, therefore limiting recombination by pinning the Fermi level close to the band edge [8,9].

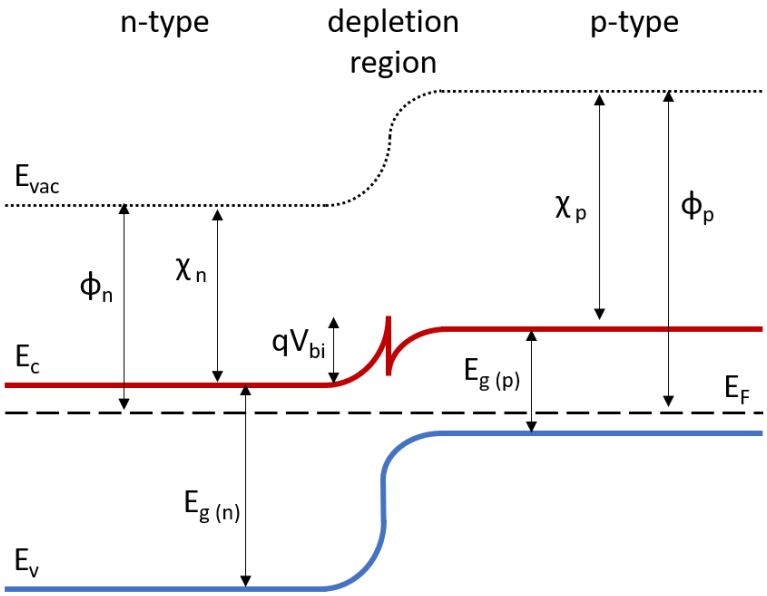

Figure 2.5: Example of a heterojunction band diagram formed between *p*-type and *n*-type layers of two different semiconductors under short circuit conditions. The electron affinity and band gap of the *n*-type (χ_n, $E_{g(n)}$) and *p*-type (χ_p, $E_{g(p)}$) layers differs for each material and therefore results in band offsets at the junction interface.

2.3.3 Schottky Junctions

When extracting charge carriers from a solar cell, an ohmic contact is desired for high efficiency to prevent carrier recombination and a parasitic voltage drop across the contact. This is facilitated by contacting *n*-type semiconductors with lower work function metals, and *p*-type semiconductors with metals of higher work function. In some instances, this may not be possible and therefore a rectifying Schottky junction is formed instead, which carriers must tunnel through to be extracted. Such junctions are described by the Schottky-Mott theory whereby an idealised semiconductor-metal contact forms a depletion region with barrier height (Φ_b) for *n*-type and *p*-type semiconductors:

$$\Phi_b(n) = \phi_{metal} - \chi_{sc} \tag{2.1}$$

$$\Phi_b(p) = (\chi_{sc} + E_g) - \phi_{metal} \tag{2.2}$$

Where χ_{sc} is the semiconductor electron affinity and ϕ_{metal} is the metal work function [10]. Figure 2.6 illustrates the band alignment expected for a *p*-type semiconductor with a low work function metal, resulting in band bending at the interface which limits hole extraction. This situation is typical for contacts to *p*-type CdTe due to a lack of metals with a suitably high work function. Whilst this qualitatively describes band bending at metal-semiconductor junctions, in practice Schottky barrier heights show a much weaker dependence on metal work function due to Fermi level pinning at surface states [11].

Although Schottky junctions are primarily relevant to solar cells due to contacting issues and considered detrimental, such a rectifying junction can be used in the active region to separate charge carriers. However, such solar cells are limited by thermionic emission and surface states which aid recombination [12].

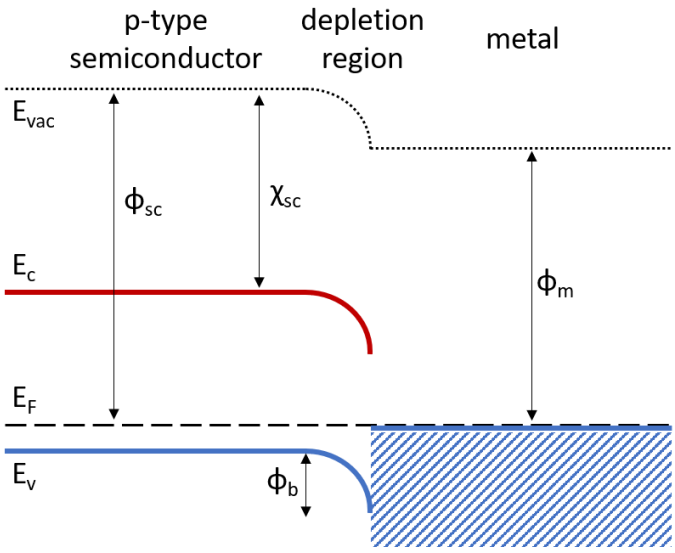

Figure 2.6: Example of a Schottky junction band diagram formed between a *p*-type semiconductor in contact with a metal of lower work function under short circuit conditions.

2.3.4 Electrostatics of p-n junctions

The formation of a depletion region in a *p-n* junction is driven by the diffusion current reaching equilibrium with the opposing drift current. The movement of majority carriers over the interface due to a chemical potential gradient results in a diffusion current and behind a region of ionised atoms close to the *p-n* junction. The positively charged ions in the *n*-type layer and the negatively charged ions of the *p*-type layer results in an electric field which sweeps minority carriers to the opposite side of the junction, resulting in a drift current. An equilibrium is reached when the diffusion and drift currents, shown in Figure 2.7b, are equal and opposite in direction and a depletion region is then formed between $x_p < x < x_n$ as shown in Figure 2.7a.

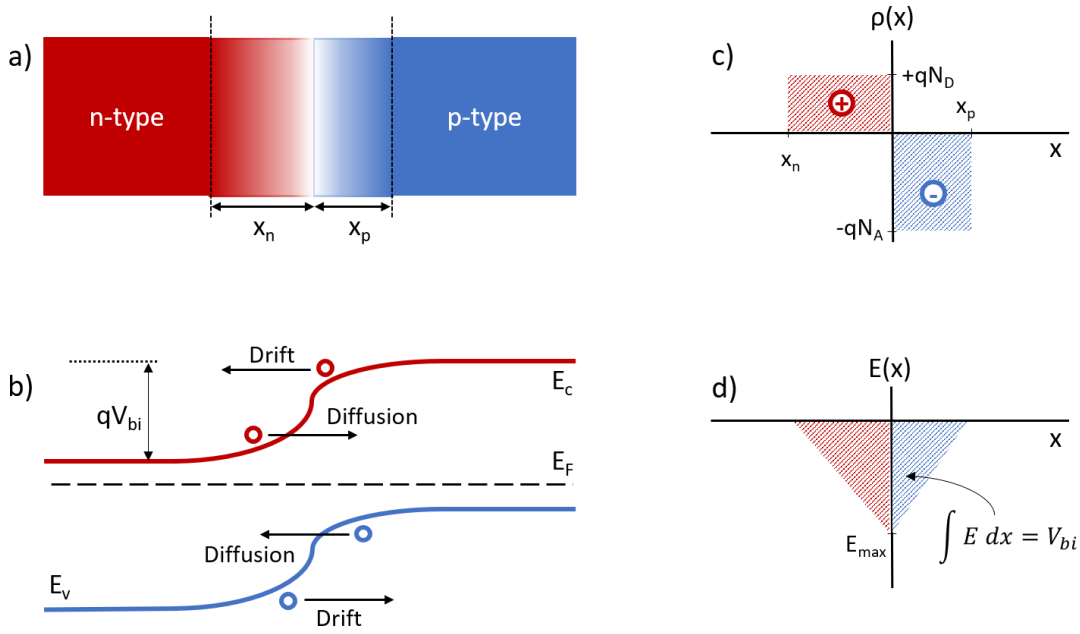

Figure 2.7: (a) schematic diagram of *p-n* junction formation and depletion region, (b) energy bands in a *p-n* junction and carrier flow with corresponding (c) charge density distribution and (d) electric field distribution

Both *n*-type and *p*-type layers are assumed to have a uniform doping profile with an abrupt junction and depletion region without free carriers as shown in Figure 2.7c. In this case, the built-in potential is determined by the difference in work function of the two layers:

$$V_{bi} = \phi_{n-type} - \phi_{p-type} = \frac{kT}{q} \ln\left(\frac{N_A\, N_D}{n_i^2}\right) \tag{2.3}$$

Where ϕ is the work function of the semiconductors, k is Boltzmann's constant, T is temperature, N_A and N_D are the acceptor and donor concentrations respectively and n_i is the

intrinsic carrier concentration. The resulting electric field is distributed across the junction, and sweeps mobile charges carriers away from the depletion region as shown in Figure 2.7d.

The width of the depletion region (W) in which there are no mobile charge carriers can be calculated by solving Poisson's equation. By assuming a one-sided junction (i.e. $N_D \gg N_A$) as is found in typical thin film solar cells, this reduces to:

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A\, N_D}\right) V_{bi}} \approx \sqrt{\frac{2\,\varepsilon_s\, V_{bi}}{q\, N_A}} \qquad (2.4)$$

Where ε_s is the dielectric permittivity of the semiconductor in which the one-sided junction resides. A forward bias applied across a *p-n* junction opposes the built-in potential leading to a reduction in overall junction potential of $V_{bi} - V_{applied}$. This lower potential barrier increases the diffusion current and therefore decreases the width of the depletion region, with current transport across the junction proceeding via the recombination of injected minority carriers. The opposite happens for reverse bias, whereby diffusion current is decreased due to an increased junction potential and the depletion region is widened, reducing current flow.

2.4 Ideal Solar cells

The addition of suitable contacts to either side of a carefully designed *p-n* junction under illumination will result in the generation and separation of electron-hole pairs and therefore in a functional solar cell. This can be modelled with an equivalent circuit diagram such as that shown in Figure 2.8 whereby a light generated current source is placed in parallel with a *p-n* junction diode. At short circuit, the light generated current (J_L) flows through the external circuit whereas at open circuit the diode current (J_D) is equal and opposite to the light generated current. Solar cells operate between these two points and in reality are subject to the effects of series (R_s) and shunt resistance (R_{sh}), however for an ideal device these are neglected (i.e. $R_{sh} = \infty$, $R_s = 0$). The impact of these resistive elements is discussed in section 2.5.4.

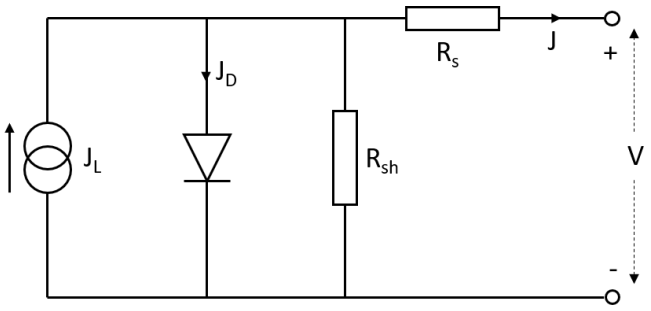

Figure 2.8: Equivalent circuit model of a solar cell under illumination whereby a photogenerated current source (J_L) is in parallel with a diode with current J_D. In the case of an ideal solar cell, it is assumed that there is no leakage current ($R_{sh} = \infty$) and no series resistance ($R_s = 0$)

2.4.1 *JV* characteristics of solar cells

The current passing through a solar cell such as that shown in Figure 2.8 in the dark (J_{dark}), neglecting the effects of series and shunt resistance, can be described as a function of applied bias by the Shockley diode equation [13]:

$$J_{dark} = J_0(e^{\frac{qV}{nkT}} - 1) \tag{2.5}$$

Where J_0 is the reverse saturation current describing the forward current flowing through the cell due to diffusion and recombination of minority carriers determined by the material properties of the diode [14], and n is the diode ideality factor [15]. When a solar cell is illuminated, current flows in the opposite direction to that which would otherwise be allowed by the p-n junction diode, resulting in a net current (J):

$$J = J_{dark} - J_L = J_0\left(e^{\frac{qV}{nkT}} - 1\right) - J_L \tag{2.6}$$

In the case of an ideal solar cell, the *JV* characteristics under illumination are the same as when in the dark offset by photogenerated current density *(J_L)*, which moves the operating point into the fourth quadrant of current-voltage diagram whereby power can be extracted. Examples of such curves are shown in Figure 2.9 with relevant device parameters marked for the light curve.

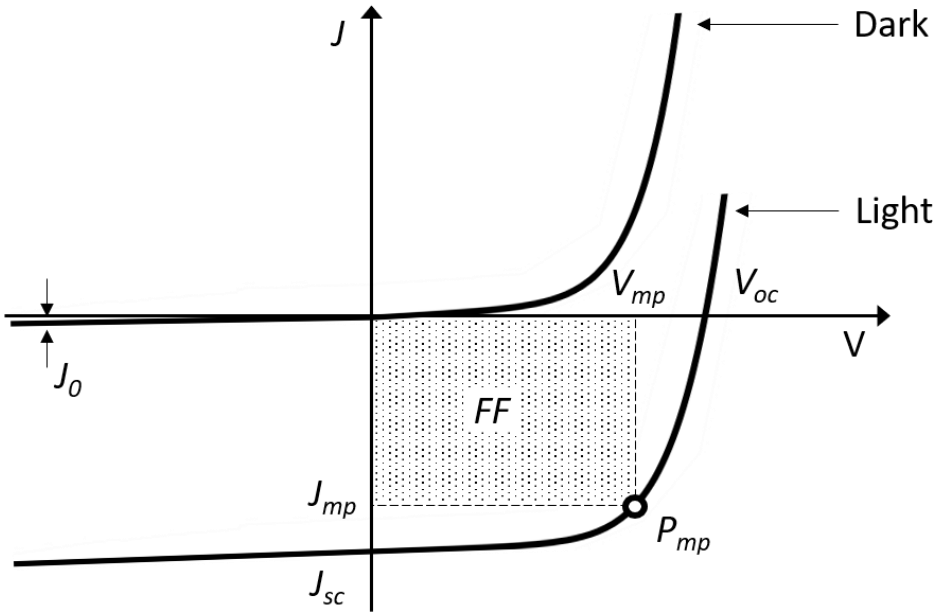

Figure 2.9: Example of ideal solar cell *JV* curves in the dark and under illumination

The performance parameters of a solar cell can be determined by measuring the *JV* characteristics under illumination, which in turn can determine the power conversion efficiency (η). Each of these parameters are briefly discussed below:

Short circuit current density (J_{sc}) is the current flowing through an external circuit connected to a solar cell under no load. In this case, the J_{dark} term is zero and therefore equation (2.6) reduces to $J_{sc} = J_L$ for an ideal solar cell, with J_{sc} being measured from the *y*-intercept of the *JV* curve. The maximum short circuit current density is determined by the number of above band gap photons incident upon the solar cell, which is in turn determined by the illumination spectrum and the band gap of the absorber layer.

Open circuit voltage (V_{oc}) is the voltage at which no current can flow through the external circuit. This represents the forward bias voltage at which the photogenerated current is equal to the dark current in the opposite direction. By setting $J = 0$ in equation (2.10 and letting $V = V_{oc}$, we define V_{oc} as:

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_L}{J_0} + 1\right) \tag{2.7}$$

Fill factor (FF) indicates how 'square' a *JV* curve is and gives the ratio of the power output of a solar cell at its maximum power point to the product of J_{sc} and V_{oc}. Since no power is extracted from solar cells operating at either short circuit or open circuit, the maximum power point exists at a J_{mp} and V_{mp} slightly below J_{sc} and V_{oc} respectively, as shown in Figure 2.9. Smaller differences between these values produce a more 'square' *JV* curve with, higher fill factor therefore higher power output. High fill factor values indicate a more ideal *JV* curve shape and lack of significant performance losses.

$$FF = \frac{J_{mp}\, V_{mp}}{J_{sc}\, V_{oc}} = \frac{P_{mp}}{J_{sc}\, V_{oc}} \tag{2.8}$$

Power conversion efficiency (η) indicates the ratio of power output from a solar cell to the power of the light incident upon the device. This is the defining metric of solar cell performance and is typically measured under standard test conditions, with AM1.5G illumination at an intensity of 1000 W/m^2 and temperature of 25 °C.

$$\eta = \frac{P_{mp}}{P_{in}} = \frac{J_{sc}\, V_{oc}\, FF}{P_{in}}, \qquad \eta_{STC} = \frac{J_{sc}\, V_{oc}\, FF}{1000\ W/m^2} \tag{2.9}$$

2.5 Losses in solar cells

Ideal solar cells are fundamentally limited in efficiency due to the principle of detailed balance [16] whereby materials that can absorb photons to create electron-hole pairs are prone to recombination as well as from spectrum losses. Real device performance is further limited by practical difficulties in realising ideal solar cell designs and the existence of finite series and shunt resistances. Practical limits on the achievable efficiency of solar cells are described below together with the effect of non-idealities on device performance.

2.5.1 Shockley-Queisser Limit

The Shockley-Queisser limit describes the maximum efficiency a single junction solar cell can achieve assuming non-concentrated sunlight whereby each photon generates a single electron-hole pair which will thermalize to the band edges. Since photons with energy below the band gap of the semiconductor will not be absorbed and photons with energy above the band gap will lose energy to thermalisation, a significant fraction of the incident energy is not utilised by single junction solar cells. Therefore the maximum efficiency requires a trade-off between high J_{sc} achieved through the use of a low band gap semiconductor which absorbs a greater fraction of the incident spectrum, and high V_{oc} where a high band gap semiconductor allows for a larger built in voltage. Furthermore, a solar cell in thermal equilibrium will emit photons as well as absorbing them. This principle of detailed balance places a lower limit on the amount of recombination that takes place in a solar cell, limiting the achievable efficiency.

Considering this, the maximum efficiency of a single junction solar cell can be calculated for a given solar spectrum as a function of the absorber band gap. The AM1.5G spectrum, shown in Figure 2.10a, is typically used to measure solar cells for terrestrial use and places an efficiency limit of 33% for a solar cell with absorber band gap of 1.4 eV as shown in Figure 2.10b. Several strategies for solar cell designs that exceed the Shockley-Queisser limit exist which are based on overcoming one of the several assumptions made. These include the use of several *p-n* junctions, concentrating sunlight, multiple exciton generation and up/downshifting the energy of incoming photons to better suit the absorber band gap.

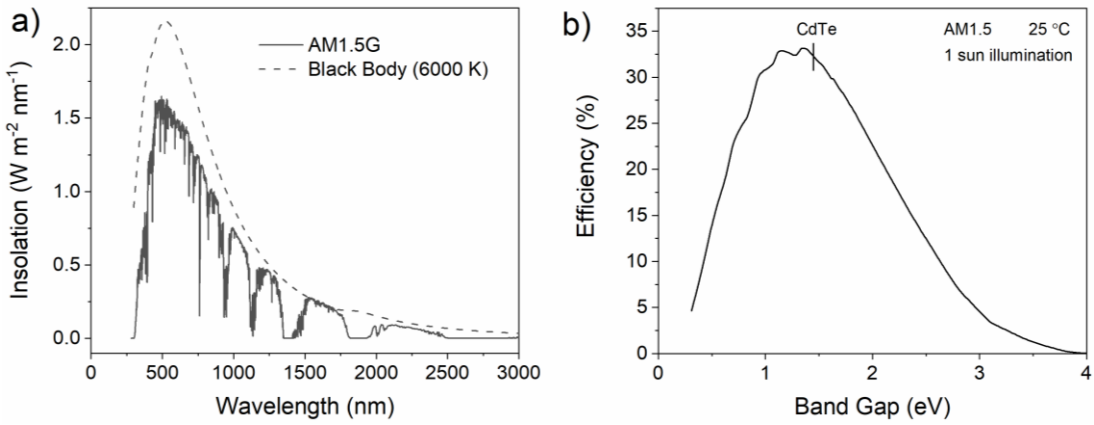

Figure 2.10: (a) AM1.5G spectrum plotted with data from ref [17] compared to spectrum emitted by a blackbody at 6000 K, and (b) the maximum theoretical efficiency of a single junction solar cell under as a function of band gap as calculated by Rühle [18]

2.5.2 Optical Losses

The Shockley-Queisser limit assumes that all above band gap photons are absorbed in the active layer of the solar cell and are efficiently collected by the electric field. In real devices, this is not always the case. Photons can be absorbed in one of the protective overlayers such as the encapsulant or glass, and reflection can occur at one of the several interfaces within a module. Electrical contacts in the form of metallic grids or transparent conductors can be sources of parasitic absorption, as well as in the high resistivity transparent layer and window layers (see section 3.4). This can be particularly challenging for heterojunction solar cells such as CdTe and CIGS where CdS is commonly used as a window layer. The relatively small band gap (~2.4 eV) and higher doping density of the layer means the electric field exists primarily within the absorber layer. Electron-hole pairs generated in the window layer are not collected efficiently and hence absorption occurring in such layers is considered parasitic absorption, with generated pairs not contributing to device photocurrent.

Absorber layers that are excessively thin either by design or due to areas of non-uniformity will also transmit some of the incoming radiation due to their finite thickness, limiting J_{sc}. The reduction in current output due to the optical losses described above can be mitigated to some extent through the use of anti-reflection coatings and texturing, whilst ensuring layers that do not contribute photocurrent are as thin and transparent as possible.

2.5.3 Recombination Losses

As mentioned in section 2.5.1, detailed balance requires that a blackbody in thermal equilibrium must emit as well as absorb radiation and therefore not all absorbed photons contribute energy due to radiative recombination. However, this describes the lower limit of recombination that exists within a solar cell, and in reality it is accompanied by non-radiative recombination. Electron-hole pairs that are not separated effectively by the *p-n* junction within an average lifetime τ will recombine, especially in the vicinity of a defect level within the absorber band gap. Defect mediated recombination occurs when states within the band gap trap charge carriers and is particularly efficient when these defect states are located close to the middle of the band gap. Such mid-gap states maximise the probability of capturing both an electron form the conduction band and hole from the valence band, resulting in non-radiative recombination. A high defect density reduces the average lifetime of minority carriers since defect states encourage the recombination of electron-hole pairs, which reduces the likelihood of carriers within the quasi-neutral region reaching the junction where they can be efficiently collected.

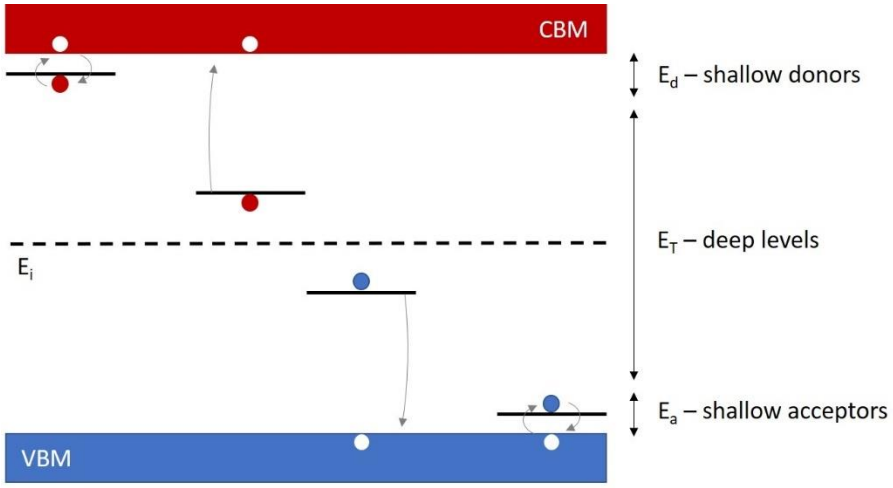

Figure 2.11: Diagram showing the energy levels associated with donor and acceptor levels involved in semiconductor doping, compared to deep level defects which contribute to non-radiative recombination of electron-hole pairs

Figure 2.11 emphasises the importance of the location of the energy level of a semiconductor impurity. Extrinsic doping requires impurities to be intentionally added to a material to increase the carrier concentration. These impurities will ideally introduce shallow dopant levels which are close (i.e. less than a few kT) to the band edges, which increases the likelihood of ionisation and therefore ensures efficient doping. In contrast, defect levels which lie deeper in the band gap can trap majority and minority charge carriers, prompting non-radiative recombination and therefore limiting carrier lifetime.

These defect states are concentrated at grain boundaries, interfaces, and point defects within the bulk material. As well as reducing photocurrent from poor collection, recombination lowers the minority carrier concentration within a semiconductor which increases the diffusion current across the *p-n* junction and therefore increases J_0. Since the open circuit voltage defines the bias at which the diffusion current is equal and opposite to the photogenerated current, it is highly sensitive to the recombination rate. Therefore, to maximise V_{oc} it is favourable to have a highly doped absorber layer with minimal impurities, large grains and passivated interfaces to maximise minority carrier lifetime and reduce the recombination rate.

2.5.4 Resistive losses

The *JV* characteristics of an ideal solar cell were described in section 2.4.1 with the assumption of infinite shunt resistance and zero series resistance, however in real devices these resistance terms are finite and can have a non-negligible impact on performance. Series resistance arises due to the bulk resistivity of the various layers and contacts within the device stack as well as resistance at the interfaces which can be influenced by potential barriers in the case of non-optimised contacts. An estimate of the series resistance (R_s) within a solar cell can be taken from the inverse of the slope of a *JV* curve close to V_{oc} as shown in Figure 2.12a. Since no net current flows at V_{oc} it is not affected by increased series resistance, which primarily affects the fill factor, although excessive series resistance can cause a decrease in current density.

Shunt resistance (R_{sh}) describes the leakage pathways in which current avoids the effects of the main diode and should be as high as possible to achieve high efficiencies. Low shunt resistances can be caused by microscopic defects such as conductive grain boundaries or pinholes in device layers which short circuit the device by providing an alternative route for current, bypassing the main junction. Low shunt resistance affects the shape of *JV* curves near short circuit resulting in a non-zero gradient as shown in Figure 2.12b and can affect both V_{oc} and J_{sc}, although again primarily limits fill factor. Including the effects of non-negligible series and shunt resistance in a solar cell leads to a modification to the Shockley diode equation:

$$J = J_{dark} - J_L = J_0\left(e^{\frac{qV}{nkT}} - 1\right) + \frac{(V - JR_s)}{R_{sh}} - J_L \qquad (2.10)$$

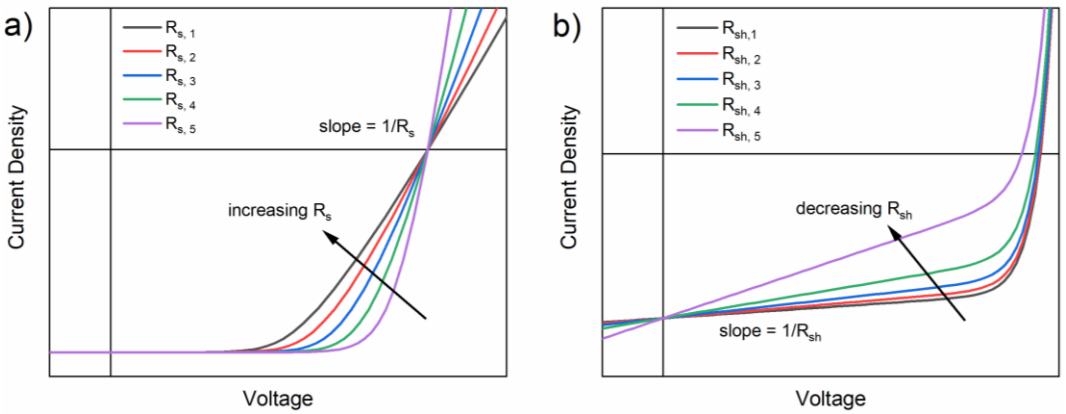

Figure 2.12: SCAPS simulations showing the effect of (a) series resistance and (b) shunt resistance on *JV* characteristics of solar cells

2.5.5 Secondary barriers

Non-ohmic contacts to solar cells can result in the formation of a Schottky barrier (as described in section 2.3.3) which produces a diode in the opposite direction to that of the main *p-n* junction. The effect of this on device performance is shown in Figure 2.13a, whereby the shape of *JV* curves is distorted in forward bias where the potential is reduced across the main junction but increased across the Schottky junction. This has a current limiting effect in forward bias referred to as 'rollover'. Since carriers must tunnel through this secondary barrier to be collected there is an increase in series resistance and therefore a reduction in fill factor. The increased likelihood of recombination at the contact due to excess uncollected carriers can also reduce V_{oc}.

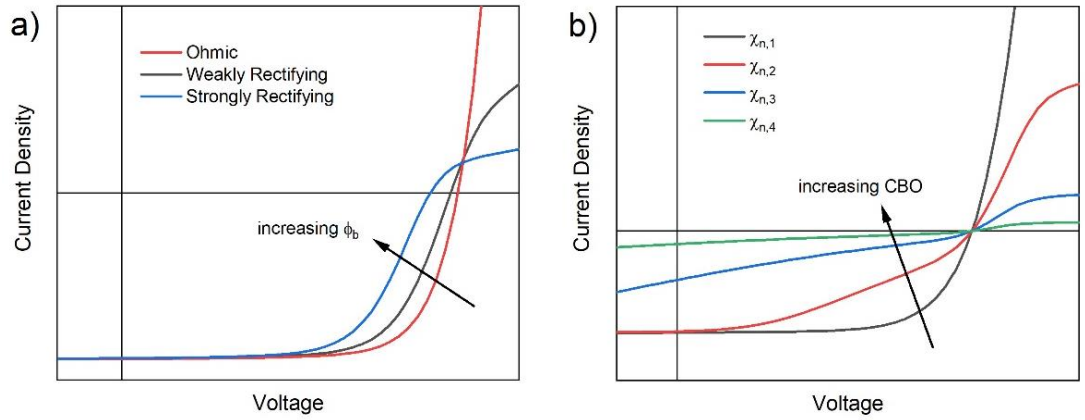

Figure 2.13: SCAPS simulations showing the effect of (a) back contact barrier and (b) a positive conduction band offset on *JV* characteristics of solar cells

Secondary barriers can exist not only at the metallic contacts of a solar cell, but also at the main *p-n* junction. If the electron affinity of semiconductors in a heterojunction are not well matched, a conduction band offset will exist which can cause a discontinuity in the band structure. Several types of conduction band alignments are shown in Figure 2.14. A negative

conduction band offset will result in a high electron density in the *n*-type layer close to a high hole concentration in the *p*-type layer and therefore encourage interfacial recombination. This reduces the built-in potential as shown in Figure 2.14d. Whilst this is detrimental to device performance, it will not cause a secondary barrier. In contrast, a positive conduction band offset can cause a spike in the conduction band. Depending on the size of the offset, this spike can act as a barrier to charge transport. Whereas a small conduction band spike (Figure 2.14b) can be beneficial by increasing type inversion and therefore preventing junction recombination at the interface, an excessively large spike (Figure 2.14a) will create a barrier to charge transport and therefore limit current even at modest biases. The effect of a positive conduction band offset and therefore spike in the conduction band is shown in Figure 2.13b whereby mismatched electron affinities create an 'S' shape in the *JV* curve due to charge accumulation at the interface, severely limiting J_{sc} and fill factor.

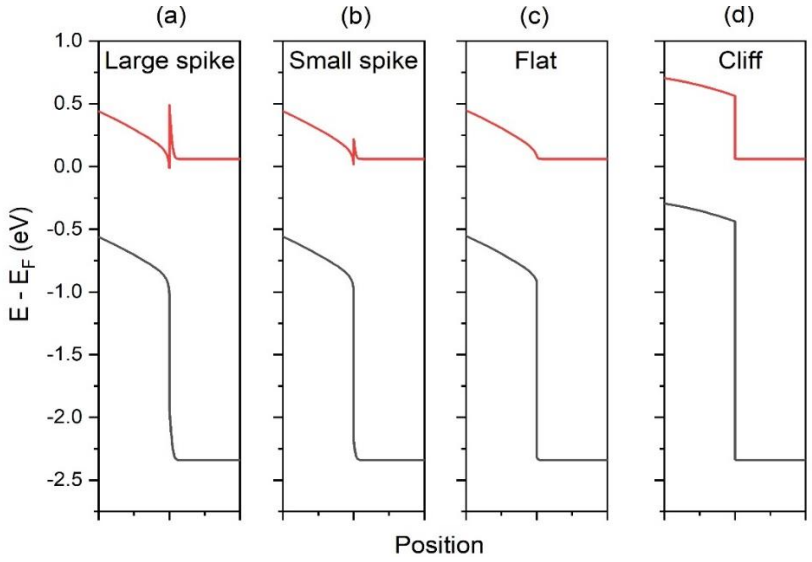

Figure 2.14: SCAPS simulations showing the valence band and conduction band alignment at the interface of a heterojunction solar cell whereby the electron affinity of the window layer is varied to produce an (a) large spike, (b) small spike, (c) flat and (d) cliff type conduction band offset.

2.6 Summary

The physical principles underlying the formation and operation of solar cells have been explained here, from the fundamental properties of semiconductors through to the current-voltage characteristics of finished devices. The limits of maximum efficiency for a single junction solar cell are shown to display a strong dependence on the absorber band gap, balancing requirements for both high current and voltage for maximum power output. The optimum band gap falls in the range ~ 1 – 1.5 eV, making CdTe a suitable absorber layer with potential to reach ~30% efficiency. Several non-idealities of solar cells have been described to explain why Shockley-Queisser limits have not been reached and how this can be diagnosed from *JV* measurements.

2.7 References

1. Becquerel, A. E. Memoire sur les effects d´electriques produits sous l´influence des rayons solaires. *Annalen der Physick und Chemie* **54**, (1841).
2. Adams, W. G. & Day, R. E. The action of light on selenium. *Proceedings of the Royal Society of London* **25**, 113–117 (1877).
3. Chapin, D. M., Fuller, C. S. & Pearson, G. L. A new silicon p-n junction photocell for converting solar radiation into electrical power. *Journal of Applied Physics* vol. 25 676–677 (1954).
4. Sze, S. M. & Ng, K. K. *Physics of semiconductor devices*. (Wiley-Interscience, 2007).
5. Nelson, J. *The Physics of Solar Cells*. (Imperial College Press, 2003).
6. Würfel, P. & Würfel, U. Physics of Solar Cells From Basic Principles to Advanced Concepts. (Wiley-VCH, 2016).
7. Anderson, R. L. Germanium-gallium arsenide heterojunctions. *IBM Journal of Research and Development* **4**, 283–287 (1960).
8. Klenk, R. Characterisation and modelling of chalcopyrite solar cells. *Thin Solid Films* **387**, 135–140 (2001).
9. Scheer, R. & Schock, H.-W. Theory of chalcogenide solar cells. in *Chalcogenide Photovoltaics: Physics, Technologies, and Thin Film Devices* (Wiley-VCH Verlag GmbH & Co. KGaA, 2011). doi:10.1002/9783527633708.
10. Tyagi, M. S. Physics of schottky barrier junctions. in *Metal-Semiconductor Schottky Barrier Junctions and Their Applications* 1–60 (Springer US, 1984).
11. Bardeen, J. Surface states and rectification at a metal semi-conductor contact. *Physical Review* **71**, 717–727 (1947).
12. Landsberg, P. T. & Klimpke, C. Theory of the schottky barrier solar cell. *Proceedings of the Royal Society of London. Series A, Mathematical and Physical Sciences* **354**, 101–118 (1977).
13. Shockley, W. The theory of p-n junctions in semiconductors and p-n junction transistors. *Bell System Technical Journal* **28**, 435–489 (1949).
14. Cuevas, A. The recombination parameter J_0. in *Energy Procedia* vol. 55 53–62 (Elsevier Ltd, 2014).
15. Sah, C. T., Noyce, R. N. & Shockley, W. Carrier generation and recombination in p-n junctions and p-n junction characteristics. *Proceedings of the IRE* **45**, 1228–1243 (1957).
16. Shockley, W. & Queisser, H. J. Detailed balance limit of efficiency of p-n junction solar cells. *Journal of Applied Physics* **32**, 510–519 (1961).
17. ASTM Standard G-173. Reference Air Mass 1.5 Spectra. (2003).
18. Rühle, S. Tabulated values of the Shockley-Queisser limit for single junction solar cells. *Solar Energy* **130**, 139–147 (2016).

Chapter 3

Development of CdTe solar cells

3.1 Introduction

As a result of its high absorption coefficient and near ideal direct band gap CdTe has been investigated as a photovoltaic material since the 1960s [1]. Adirovich et al reported the first CdS/CdTe heterojunction thin film solar cell in 1969 [2], which became the standard structure for the following 40 years. By identifying the role of impurities such as oxygen, copper, and chlorine, developing a post growth $CdCl_2$ treatment, and optimising front and back contacts the efficiency was gradually improved from 6% in 1972 [3] to 16.5% in 2001 [4]. With no further increases observed in the following decade, new device architectures beyond CdS/CdTe have been explored since 2011, leading to further efficiency gains [5] as shown in Figure 3.1a. First Solar currently hold the record cell efficiency at 22.1% [6] achieved through a combination of selenium grading in the absorber layer and a reduction in parasitic absorption in the window layer, though the details of the exact device structure remain commercially sensitive. Translating these cell level advances into CdTe modules has enabled a record efficiency of 19%, which is competitive with typical polycrystalline silicon modules and narrows the gap to single crystal silicon.

By leveraging the inherent advantages of continuous in-line production of monolithically integrated modules, CdTe has been able to outcompete silicon PV in price despite being well behind in the experience curve shown in Figure 3.1b. This shows the average selling price of electricity generated by different PV technologies compared to the total manufactured capacity, and demonstrates that thin film PV has managed to achieve a similar or lower price per watt despite manufacturing a relatively small volume of modules. Therefore, as manufacturing volume increases, economies of scale are expected to allow further cost reductions, whilst continuous improvements to the underlying technology continue to increase CdTe module efficiency.

This chapter describes the key layers and processing steps involved in the development of CdTe solar cells.

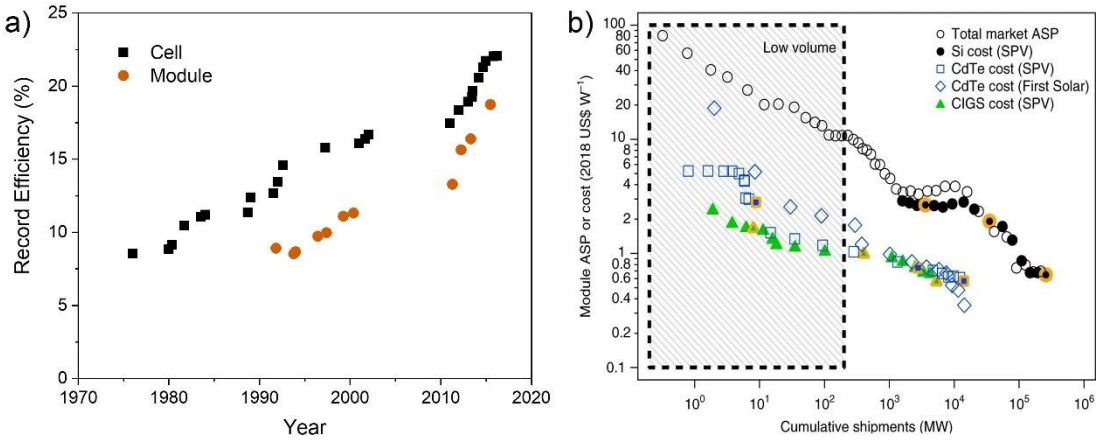

Figure 3.1: (a) Historical record efficiency of CdTe cells and modules with data from NREL efficiency charts [7,8], and (b) average cost per watt of electricity for different photovoltaic technologies as a function of manufacturing capacity, reproduced from ref [9]

3.2 Device Structure

CdTe solar cells are typically made in the superstrate configuration, whereby layers are deposited sequentially onto a transparent substrate through which light enters to reach the *p-n* junction. The substrate configuration, in which the deposition sequence in reversed, is far less common and hindered by the requirement for an ohmic back contact that is stable to high processing temperatures. Although challenging, the substrate geometry can offer greater control over junction formation and reasonable efficiencies have been achieved [10]. Devices made in this work are prepared in superstrate configuration, and an example of a typical CdTe solar cell structure is shown in Figure 3.2.

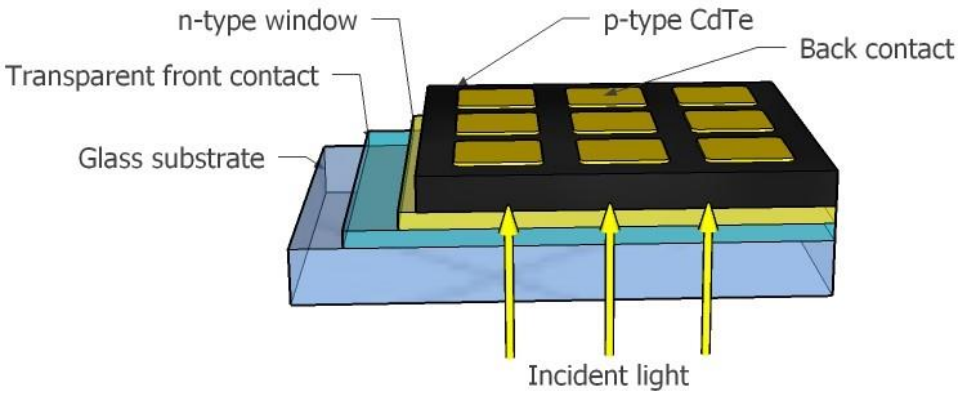

Figure 3.2: Structure of a typical CdTe solar cell in superstrate configuration

3.3 Substrate and TCO

The choice of substrate for CdTe solar cells is limited by the requirement to withstand high processing temperatures (>500°C) and possess a suitable thermal expansion coefficient. The substrate must also be transparent across the solar spectrum, and practical considerations dictate low cost and greater than 20-year environmental durability. For high processing temperatures encountered in research high quality aluminosilicate or borosilicate glass can be used, however lower cost soda lime glass (SLG) is more suited to large scale manufacturing. Impurities which are purposefully added to lower the glass processing temperature such as sodium and magnesium can diffuse into the active layers of the solar cell during deposition, and therefore diffusion barrier layers such as SiO_2 are required to inhibit this. Unintentional impurities can also reduce light transmission therefore a low-iron content is typically required. Anti-reflection coatings, which can be applied to match refractive indexes at interfaces and therefore reduce reflection losses, are subject to the same engineering and economical constraints as the glass itself.

Transparent conducting materials are deposited onto the substrate to collect current whilst allowing maximum light transmission into the absorber layer. To obtain these normally mutually exclusive properties of electrical conductivity and optical transparency, wide band gap semiconductors are degenerately doped to move the fermi level outside of the band gap and therefore allow conductivity. Fluorine doped tin oxide (FTO) is commonly used in CdTe solar cells, with thin and therefore transparent films offering reasonable conductivity. It is chemically and thermally stable and therefore tolerant to high temperature deposition of the subsequent films in the device stack. It is also industrially scalable, and already manufactured in large quantities via a float line chemical vapour deposition process for numerous applications such as energy efficient windows. Tin doped indium oxide (ITO) is also commonly used, offering lower sheet resistance for a given thickness thereby allowing thinner and more transparent films for the same conductivity. However, this can be thermally unstable at typical CdTe processing temperatures and therefore requires a diffusion blocking layer whilst the presence of indium, a rare-earth metal, is undesirable for large scale manufacturing.

Other transparent conducting oxides (TCOs) are currently being explored, with Cd_2SnO_4 (CTO) notable for its use in previous record devices [11]. This can offer higher transparency and conductivity than FTO layers. However, the hygroscopic nature of CTO layers, which require high processing temperatures (>600°C) for optimal film properties and therefore not suitable for use with SLG substrates, may limit scalability. Aluminium doped zinc oxide (AZO) layers are also commonly used in CdTe device fabrication, however can degrade during subsequent device processing steps [12] and are therefore limited to low temperature CdTe depositions.

FTO remains the standard choice and is used in the current highest reported efficiency device with a publicly available cell structure [13]. Commercially available soda lime glass substrates are used in this work, with FTO films deposited by the manufacturer via atmospheric pressure chemical vapour deposition.

3.4 Window layer

A high surface recombination velocity combined with a large absorption coefficient means that CdTe homojunctions are not suitable for PV applications, since carrier generation occurs close to a highly defective surface. To prevent this a heterojunction is formed with a more transparent *n*-type window layer, thereby shifting the absorption profile into the CdTe where carriers can be effectively separated by the internal electric field [14]. As well as practical considerations, such as the ability to withstand high processing temperatures, toxicity and long term stability, the design requirements of an ideal heterojunction partner includes (i) a small, positive conduction band offset for optimal carrier extraction, (ii) high doping density to ensure type inversion and (iii) a large band gap to prevent parasitic absorption [15,16].

3.4.1 CdS based window layers (CdZnS, CdS:O etc)

CdS films have historically been the most common choice of window layer for CdTe solar cells as well as other thin film technologies [17]. Native *n*-type doping is afforded by sulphur vacancies [18] and therefore does not require control over extrinsic dopants. Carrier concentrations above 10^{16} cm^{-3} are commonly achieved from a variety of growth methods [14], typically resulting in a one-sided junction with CdTe. A lattice mismatch of ~10% means that intermixing between CdS and CdTe to form CdS_yTe_{1-y} and $CdTe_xS_{1-x}$ phases has been considered vital either during deposition or chlorine activation to grade the lattice constant and alleviate interfacial strain. However, recent work has demonstrated single crystal CdTe solar cells with V_{oc} above 950 mV in spite of an abrupt junction with no detectable interdiffusion, and it was belatedly realised that lattice mismatch alone is unlikely to be the limiting factor for open circuit voltage [19]. Whilst a band gap of 2.4 eV is reasonably transparent to most of the solar spectrum, photons below 515 nm can be absorbed in the CdS layer where they are not effectively collected by the one-sided junction. This parasitic absorption limits the maximum current output and several strategies have been employed to increase the CdS band gap.

Alloying with higher band gap materials such as ZnS allows the band gap to be tuned and therefore increases the photon flux reaching the CdTe layer. However, this is typically accompanied by an increase in the resistivity of the window layer and a lower doping density, limiting the tolerable Zn content in alloyed $Cd_xZn_{1-x}S$ films which subsequently limits spectral response [20].

Oxygenation of CdS films to produce CdS:O allows the formation of SO_x complexes. This increases the optical band gap due to quantum confinement effects within CdS nanocrystals [21]. This increased band gap results in less parasitic absorption within the window layer and therefore an improved blue response in EQE curves, thereby increasing current output of CdTe/CdS:O devices as shown in Figure 3.3. This increase in window layer band gap not only increases J_{sc} due to improved optical transparency, but V_{oc} and fill factor can be increased due to an improvement in band alignment with CdTe [22] despite increased film resistivity. CdS has a -0.1 eV conduction band offset resulting in a cliff-like interface [23], which is improved as the electron affinity of CdS:O gradually increases with oxygen content. Although the increased band gap of CdS:O allows a thicker window layer whilst maintaining transparency, these films can recrystalise forming a bilayer following heat treatment and eventually revert back to CdS [24]. Devices incorporating CdS:O window layers typical also require the inclusion of a high resistivity transparent (HRT) layer deposited between the TCO and window layer for optimal performance [25].

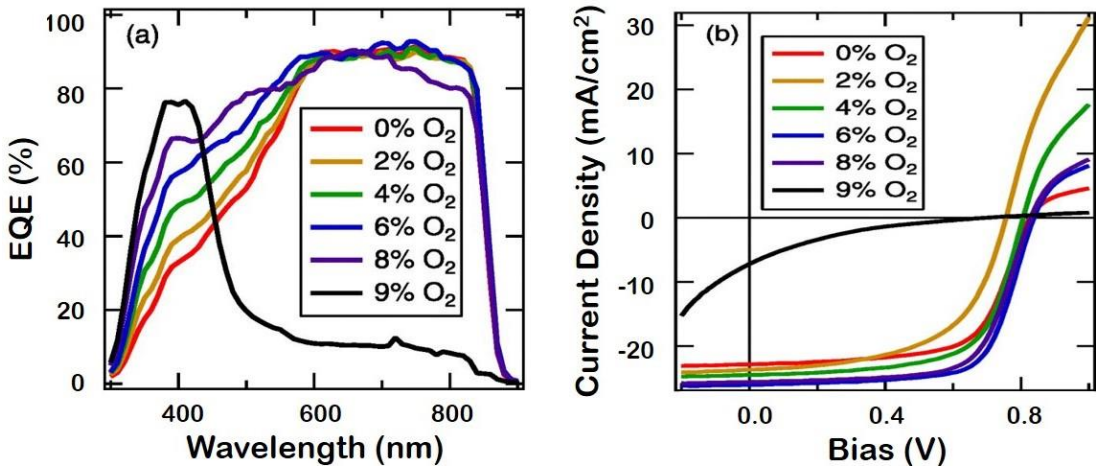

Figure 3.3: Effect of oxygen partial pressure in the CdS sputtering ambient on the (a) EQE and (b) *JV* performance of CdS:O/CdTe solar cells, reproduced from ref [26]

High Resistivity Transparent (HRT) Layers:

The parasitic absorption due to the presence of CdS in CdTe solar cells can be mitigated by simply reducing the thickness of the CdS layer, however below a critical thickness the open circuit voltage and fill factor are severely impacted. This can be seen in Figure 3.4 whereby the efficiency of CdS/CdTe devices is reduced below 100 nm despite an increase in J_{sc}. This critical thickness can be reduced, and performance improved with the inclusion of an HRT layer as shown below for HRT/CdS/CdTe devices. Wide band gap semiconductors with resistivity between that of the TCO and CdS layer are used as HRT buffer layers, typically undoped oxides of tin or zinc [27].

These were originally employed to overcome the practical issue of depositing CdS films sufficiently thin without the formation of pinholes, with the increased ohmic resistance of the HRT layer preventing direct contact between CdTe and the TCO which would result in a weak diode. However, more recent studies have clarified the dominant effect to be an improved band alignment at the TCO/CdS interface, which is most noticeable for thin CdS layers [28].

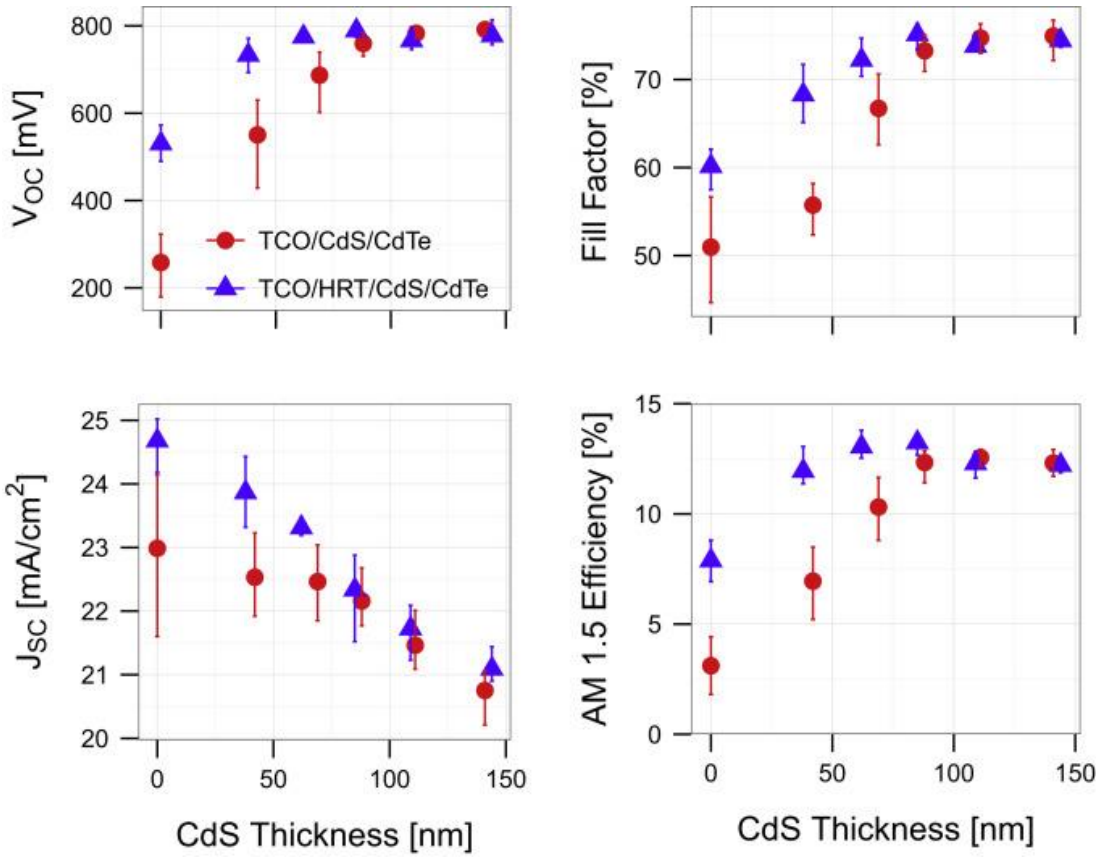

Figure 3.4: Performance parameters for devices with and without a HRT layer as a function of CdS thickness. The inclusion of a HRT layer allows the thickness of the CdS window layer to be reduced further than devices without a HRT layer without affecting V_{oc} and fill factor, reproduced from ref [27]

3.4.2 Alternative window layers

An improved understanding of the importance of band alignment has eventually allowed for the complete replacement of the CdS layer with more transparent alternatives with a suitably aligned conduction band offset [27]. A range of window layers have been assessed such as ZnSe [29], TiO_2 [30], SnO_2 [31] and ZnO [32]. The most successful alternative has been $Mg_xZn_{1-x}O$ (MZO) which replaces both CdS and the HRT layer and is described in detail below. SnO_2 is also reviewed as a potential window layer given its use in this work.

Magnesium Zinc Oxide (MZO):

The electron affinity of ZnO is higher than optimal for a heterojunction with CdTe, leading to a large cliff-type band alignment which reduces the built-in voltage. Alloying ZnO with MgO allows the band gap and electron affinity to be tuned such that a flat or small spike band alignment can be obtained. $Mg_xZn_{1-x}O$ has proven to be a highly transparent window layer capable of maintaining a V_{oc} comparable to that of CdS, but with reduced optical losses [27]. Varying the Mg content in MZO window layers provides an ideal platform to test the effect of band alignment on built in voltage, with significant deviation from a flat conduction band quickly reducing performance [27].

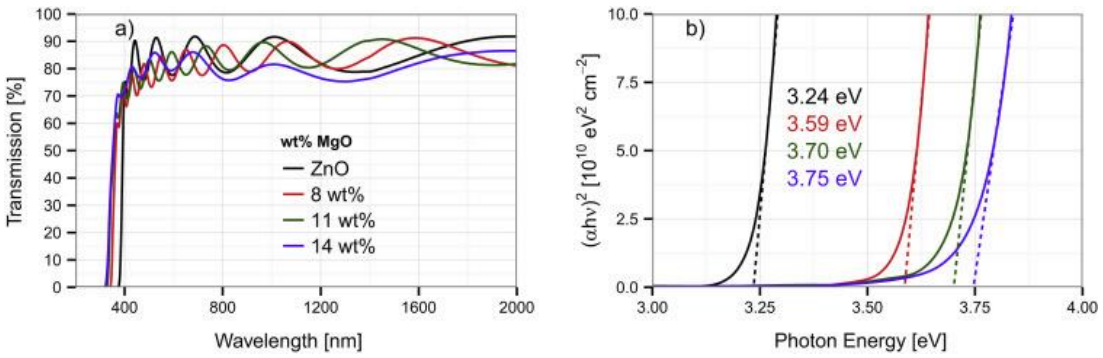

Figure 3.5: Effect of varying Mg composition in $Mg_xZn_{1-x}O$ films on the optical band gap, as shown from transmission spectra and Tauc plots. Reproduced from ref [27]

Several labs have though reported difficulties in incorporating MZO into their device structure due to the appearance of secondary barrier like effects resembling 'S' shapes in *JV* curves (see section 2.5.5), which drastically lowers the fill factor [27]. This is attributed to a large spike in the conduction band which inhibits electron transport, but may also be due to excessive resistivity of the MZO. Several strategies to overcome this have been reported by various authors [27,33,34], with different methods presumably having similar effects such as suitable adjustment of the work function or decreasing resistivity. Whilst a high doping density is desirable for a window layer to pin the Fermi level near the conduction band at the interface,

values for MZO are not commonly reported in the literature. Instead it is noted that high resistivity in comparison to CdS prevents measurement [27]. There are also reports of sensitivity of MZO layers to moisture due to the presence of hygroscopic MgO [35], which may pose an issue for commercialisation. Therefore, whilst MZO has been shown to effectively replace CdS as a widow layer and demonstrated an improved understanding of CdTe solar cell design, it is not necessarily the optimal heterojunction partner. Other potential window layers therefore remain worthy of investigation.

Tin (IV) Oxide:

Since SnO_2:F is already a common and mass produced choice of TCO for CdTe solar cells, SnO_2 is an appealing choice of window layer for large scale manufacturing. A fundamental band gap of 3.6eV means it is transparent across the solar spectrum and is natively *n*-type with nominally undoped carrier concentrations up to 10^{21} cm^{-3} [36], although it remains unclear whether the source of conductivity arises from oxygen vacancies, tin interstitial or hydrogen impurities [3738]. The electron affinity of SnO_2 is slightly higher than that of CdS [39], reported both theoretically and experimentally to be around 4.5 eV [40,41] which should result in a flat conduction band alignment. There are experimentally measured deviations from this [27] which may result from strong sensitivity of the surface to species such as oxygen [42]. This sensitivity can result in significant variations in work function depending on processing conditions and impurities, meaning controllably lowering the Fermi level below the conduction band minimum can be challenging [43] and therefore careful consideration is required to ensure an effective band alignment with CdTe [44].

Despite a seemingly promising band alignment with a highly transparent and frequently used semiconductor, there are few reports of SnO_2/CdTe heterojunction solar cells. Several authors compare FTO/CdTe junctions to the standard CdS/CdTe, with low efficiency due to degenerative doping of the TCO causing a cliff-like band alignment [45]. Nominally undoped SnO_2/CdTe junctions typically perform better as the Fermi level is closer to the conduction band allowing an improved alignment, however the voltage is still adversely affected, with junction quality being between that of CdS and FTO [46]. Recent reports of high efficiency CdTe based devices with efficiency above 19% combine a SnO_2 heterojunction with a selenium alloyed CdTe layer, whereby small amounts of selenium lowers the band gap of CdTe which might improve the band alignment [47]. At present, there still remains a lack of understanding as to how the doping level, surface work function and selenium grading of the CdTe layer influence device performance.

3.5 Absorber layer

CdTe has an optical absorption coefficient above 10^4 cm^{-1} across most of the solar spectrum, and therefore nearly all light with energy above its 1.45eV direct band gap is absorbed within the first 2 μm, allowing the active layer of devices to be orders of magnitude thinner than for crystalline silicon solar cells. In practice, slightly thicker CdTe layers of around 4 -10 μm are often used to ensure suitable uniformity, especially in research labs, but thinner absorber layers can offer lower series resistance whilst improving material utilisation. Although the microstructure of as deposited CdTe films varies significantly [48], the final device efficiency is remarkably tolerant to a range of deposition methods. High temperature growth methods such as vapour transport deposition are favoured for the most efficient devices [13], however the ubiquitous chlorine activation step passivates and recrystalises highly defective films to form suitable quality layers regardless of deposition route. A combination of chlorine treatment and selenium grading have recently allowed devices with evaporated CdTe layers to exceed 19% efficiency [47], despite room temperature deposition of the absorber layer.

3.5.1 Grain boundaries

A major advantage of thin film CdTe photovoltaics is the possibility of rapid deposition rates suitable for large volume manufacturing, however this produces polycrystalline films with a high density of grain boundaries. Debate exists over whether grain boundaries are beneficial or harmful to device efficiency. It is typically assumed that these interfaces between single crystal grains are expected to have a high density of dangling bonds which can act as recombination centres and therefore limit carrier lifetime. This is supported by higher V_{oc} attained in single crystal CdTe devices [49], correlations of increased lifetime and device efficiency with grain size [50], and luminescence studies which imply increased levels of non-radiative recombination at grain boundaries that is supressed but not eliminated with chlorine treatment [51].

However, EBIC [52] and scanning probe microscopy measurements [53–55] support the theory that grain boundaries may in fact be beneficial, enhancing collection by producing local electric fields that aid the separation and transport of carriers. Higher photocurrent at grain boundaries is attributed to reduced *p*-type doping inducing band bending which acts as a barrier for holes, thereby selectively aiding electron transport. It is worth noting that these techniques do not measure devices in operating conditions and therefore whilst current collection may be enhanced at short circuit where grain boundary potentials will have maximum impact, devices operate in forward bias close to open circuit. The same grain boundary potential that may

enhance photocurrent collection will result in more equal electron/hole concentration in the vicinity of mid-gap defect levels that aid recombination. As demonstrated for CIGSe solar cells, any potential improvement in current density afforded by charged grain boundaries is likely to be more than offset by a reduced voltage [56].

Grain boundaries have a complex defect chemistry due to a large, negative segregation energy for many common elements [57], which results in distributions similar to Figure 3.6 whereby the impurity concentration is higher at grain boundaries compared to the grain interior. Incorporation of chlorine and selenium into the CdTe layer have proven vital in recent efficiency advances [58,59], and grain boundaries offer pathways for rapid diffusion throughout the absorber layer. This is beneficial for device performance since both Cl and Se have a defect passivating effect in CdTe. However, intentionally added dopants also tend to segregate at grain boundaries thereby limiting the doping density and lowering the activation ratio, as well as acting as a reservoir for non-intentional impurities such as sodium. Sulphur rich grain boundaries are often observed due to out diffusion from CdS window layers during device processing.

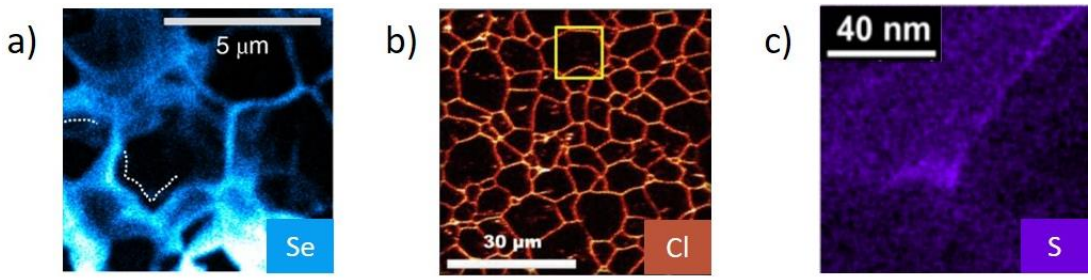

Figure 3.6: Examples of elemental maps of (a) selenium, (b) chlorine and (c) sulphur for $CdSe_xTe_{1-x}$ and CdTe films, showing high concentration of grain boundaries compared to grain interior. Reproduced from refs [58–60]

Slow, high temperature growth conditions typically result in a large grain size and therefore are used in record devices as well as commercially [13], although the recrystallization that occurs during chlorine treatment (see section 3.6) means low temperature growth methods are also acceptable. As well as the total length of grain boundaries within a polycrystalline solar cell, their orientation relative to both the substrate and to neighbouring grains can also play an important role in limiting recombination, with high angle ($\Sigma > 3$) grain boundaries running parallel to the junction being particularly undesirable [61,62].

3.5.2 Band gap grading

Although the separation of photogenerated electron/hole pairs mainly takes place within the electric field of the main *p-n* junction, the low minority carrier lifetime of CdTe means that carriers can quickly recombine before they can be extracted from the quasi neutral region. A potential strategy to mitigate this is to vary the band gap of the absorber layer such that an internal electric field exists which can help carriers drift towards their respective contacts. This approach is routinely used for CIGS solar cells [63] whereby a graded gallium composition results in an expanded band gap towards the back surface which is expected to repel electrons thereby preventing recombination. Early efforts to vary the band gap of CdTe solar cells focused on alloys with Mg and Zn which increase the conduction band minimum and were therefore expected to act as an electron back reflector [64]. However, a tendency to segregate and form volatile compounds during chlorine activation means they are difficult to incorporate into the absorber layer, instead being more suited to form highly doped contact layers as described in section 3.8.

Alloying selenium into CdTe has become an increasingly popular route to controllably vary the band gap of the resulting $CdSe_xTe_{1-x}$ layer. Whilst the band gap of CdSe is higher than that of CdTe, the band bowing effect allows for solid solutions of the two semiconductors to form a 1.38 eV band gap phase which is lower than either of its constituents [23], as show in Figure 3.7a. A graded selenium profile in the absorber layer will therefore result in a graded band gap which should result in more efficient charge collection. In addition to the graded band gap, alloying selenium allows for collection of longer wavelength photons by shifting the minimum absorber band gap closer to the ideal value of 1.34 eV which can increase current output by more than 2 mA cm^{-2} [65]. This can be seen in Figure 3.7b whereby increasing the selenium content at the front of the device shifts the absorption edge towards longer wavelengths in external quantum efficiency measurements.

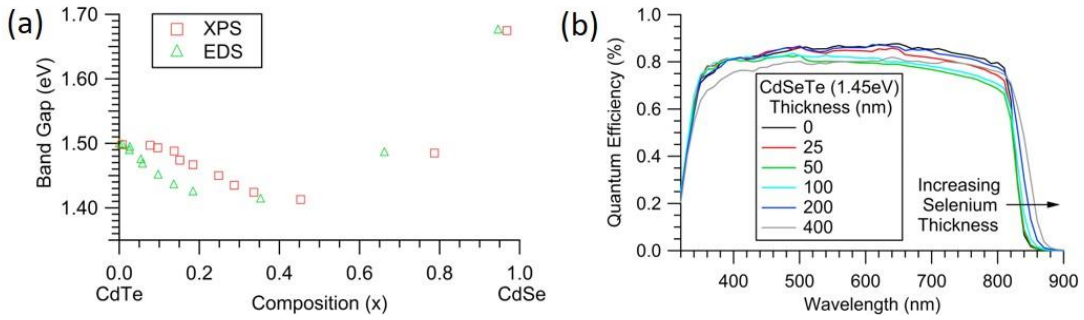

Figure 3.7: (a) Variation of band gap of $CdSe_xTe_{1-x}$ layers with selenium content, and (b) EQE of devices with different $CdSe_xTe_{1-x}$ layer thickness at the front of the device, reproduced from ref [66]

The open circuit voltage of these devices is typically maintained or improved despite the lower band gap. This has been attributed to suppressed recombination, not only by the graded electric field, but also by selenium induced passivation of defects resulting in a fundamentally better optoelectronic material [58]. This device structure has led to increases in carrier lifetime far in excess than reported for CdTe alone [67] as well as higher efficiencies. The $CdSe_xTe_{1-x}$ layer is commonly formed by sequential deposition of CdSe and CdTe followed by an annealing step encourage interdiffusion. Alternatively, directly co-sublimating either from a mixed powder or dual source CSS allows for precise control over the composition gradient of the absorber layer whilst maintaining high deposition rates of large grain material [66]. The addition of a $CdSe_xTe_{1-x}$ layer at the front interface has rapidly become the new standard for CdTe based devices.

3.6 Chlorine treatment

Polycrystalline CdTe films are not suitable for high efficiency solar cells immediately after deposition due to a high density of deep gap states which aid non-radiative recombination. These gap states are primarily found at grain boundaries whereby the termination of the repeating lattice structure produces dangling bonds. The atomic arrangement that results from this can lead to a density of states within the energy gap of bulk CdTe depending on the degree of misorientation between grains [57]. The harmful effects of these grain boundaries can be inhibited by either reducing their density (i.e. increase grain size) or limiting their ability to cause recombination (i.e. passivation). The chlorine activation treatment, which is used in all high efficiency polycrystalline CdTe solar cells, can contribute to both effects. To do this CdTe films are exposed to a chlorine source, achieved in several ways as described below, and heated to around 400°C. This allows the chlorine to redistribute throughout the device, residing primarily at grain boundaries due to a strongly negative segregation coefficient [68].

The primary effect of the chlorine treatment is chemical modification of grain boundaries to shift mid-gap states closer to the band edges or outside of the band gap entirely, thereby reducing or eliminating the excess recombination for most grain boundary types [61]. Chlorine is also expected to passivate bulk defects, in particular the mid-gap V_{Te} [69] which is expected to be an efficient recombination centre. In addition, the phase diagram for the CdTe-$CdCl_2$ system has a eutectic point at a temperature of 505°C for compositions with 74 mol. % $CdCl_2$ and therefore grain boundary passivation is accompanied by recrystallization at typical chlorine treatment temperatures [70]. Since this recrystallization is driven by the lattice strain energy, small grain CdTe films tend to undergo grain growth whereas large grained material

does not, although low formation energy defects such as stacking faults are removed by chlorine treatment regardless of the initial microstructure [71]. Furthermore, intermixing between the CdS and CdTe layers is enhanced upon chlorine treatment which can relax interfacial strain due to a ~10% lattice mismatch, and combined with increased *p*-type doping via the formation of V_{Cd}-Cl_{Te} complexes allows for the activation of the photovoltaic junction [72]. The chlorine treatment process must therefore be optimised to benefit from all these effects whilst avoiding over treatment which can delaminate films. Details of specific treatment options are detailed below.

Cadmium chloride treatment

The importance of chlorine in CdTe solar cells was first demonstrated through the use of $CdCl_2$ as a sintering aid for CdS deposition [73], which led to the discovery of the now-ubiquitous activation treatment. Substantial efficiency increases upon heating in the presence of $CdCl_2$ led to enormous efforts to understand the role and importance of chlorine in CdTe [74]. The $CdCl_2$ treatment is performed either in air or under a controlled atmosphere with specific O_2 partial pressure, as both chlorine and oxygen predicted to have a passivating effect [57,75], although oxygen in isolation does not yield the same performance increases. $CdCl_2$ can be incorporated during growth or as a post deposition treatment by evaporating a layer onto the back surface, drop casting from solution in methanol or exposure to vapour at high temperature [46]. The quantity of $CdCl_2$, anneal ambient, treatment temperature and time is then optimised for best performance.

Alternative chloride treatments

Whilst a chlorine activation treatment is essential for high efficiency polycrystalline CdTe solar cells, the use of $CdCl_2$ poses safety concerns due to its toxic nature and water solubility. In an attempt to remove this from the device structure, numerous alternative chlorine treatments have been tested such as HCl [76], $ZnCl_2$ [77], HCF_2Cl [78], NaCl [79] and $MgCl_2$ [80]. These have been effective to varying extents, and in some instances can be far easier and safer to incorporate into device processing. An aqueous $MgCl_2$ solution is used for chlorine activation in this work owing to its non-toxic nature and ease of processability whilst achieving efficiencies similar to that of the standard $CdCl_2$ process [80].

3.7 Doping

CdTe is an amphoteric semiconductor and therefore there are many potential dopants which can alter its electronic performance, however given typical n^+/p structure used for solar cells, only *p*-type dopants will be focused on here. Effective doping strategies need to balance requirements of both high hole density and long carrier lifetimes, both of which are simultaneously required to enable high V_{oc} [81].

3.7.1 Intrinsic doping

The stoichiometry of CdTe depends upon the growth conditions, which in turn determines the level of intrinsic doping of films. In general, low temperature deposition results in Cd rich films, whereas films grown at high temperatures are increasingly Te rich irrespective of growth pressure [82]. The nature of intrinsic doping in CdTe has proven challenging to study reliably due to its low mobility of as-deposited films, self-compensation effects and defect complexes, and is further complicated by the presence unintentional impurities [83].

Tellurium rich growth conditions have long been favoured to minimise the number of Te vacancies, which have been predicted to act as mid-gap recombination centres [69]. This also promotes native *p*-type doping by the formation of V_{Cd} located around 0.18 eV and 0.26 eV above the VBM for the single and double charged acceptor states respectively [82]. However, updated DFT calculations replacing the LDA functional with HSE06 as well as two-photon TRPL measurements suggest a Cd rich composition is in fact more suitable for maintaining long carrier lifetimes since the Te_i and Te_{Cd} defects, which readily form in tellurium rich CdTe, are lifetime limiting defects [84]. This indicates that Cd rich growth may in fact be optimal for long carrier lifetimes. Nonetheless, extrinsic cation site doping is aided by tellurium rich growth and therefore this must be balanced with increasing hole density.

3.7.2 Extrinsic doping

The relatively deep lying acceptor states of intrinsic defects in CdTe combined with strong self-compensation effects mean that extrinsic dopants are necessary to achieve high carrier concentrations [85]. However, limited solubility and poor activation ratios are typically observed, especially in polycrystalline films where impurities tend to segregate at grain boundaries [86]. The choice of dopant, as well as the method of incorporation, must therefore be carefully considered to achieve high doping density without compromising carrier lifetime. Several different doping approaches have been attempted, which are discussed in turn.

Group IB dopants:

An assumed tellurium rich stoichiometry, arising from consideration of both the defect structure and CdTe growth kinetics, means that *p*-type dopants occupying the cation site have historically been the standard choice, particularly focussing on copper. As a common impurity in CdTe, copper has been incorporated into devices since 1969 [87] and until recently has been essential for high efficiency devices, allowing hole densities around 10^{14} cm^{-3} to be routinely achieved. The Cu_{Cd} acceptor state is predicted to lie around 160 meV above the valence band [85]. This is shallower than previously suggested [23] and these states are found to be heavily ionised, with hole density limited instead by low solubility in CdTe which causes copper to segregate to grain boundaries, thereby limiting hole density below ~10^{15} cm^{-3} [88]. Diffusion along grain boundaries occurs far quicker than in the bulk, causing copper to segregate at the front contact where it can form deep states as well as at grain boundaries which can deteriorate junction quality [89,90]. The highly mobile nature of copper in CdTe can therefore cause long term stability issues where modules are exposed to repeated cycling of temperature and bias conditions [91]. Self-compensation further limits hole density, whilst also introducing deep defect levels which aid recombination and therefore limit carrier lifetime [92]. Other group IB dopants have been studied to a lesser extent, due to the deeper lying acceptor states of both Au and Ag [93] as well as observations of strongly enhanced degradation upon Ag doping [94].

Group IA dopants:

Group IA dopants are expected to act similarly to copper, however there are far fewer reports of their intentional incorporation into devices despite being a common impurity [95]. Both lithium and sodium have been studied in single crystal CdTe where they produce shallow acceptor levels and reach hole densities above 10^{17} cm^{-3} [96], and V_{oc} above 900 mV has been achieved by producing solar cells from CdTe:Na single crystals [97]. Replicating this in polycrystalline devices has been challenging as whilst sodium can successfully increase hole density [98], it also has caused adverse structural changes in both CdTe and CdS layers leading to poor efficiencies [98–101]. Furthermore, both Li and Na are expected to be highly mobile in CdTe, similarly to copper which could pose long term stability problems [96,97].

Heavier group IA elements would presumably be less mobile, however there have been almost no experimental or theoretical studies undertaken. Ultrathin CdTe devices deposited from colloidal nanocrystals capped with Na, K and Cs show progressively improved performance attributed to cation size, although it is unclear whether these alkali metal have an effect on the hole density [102]. The effect of group IA elements in CdTe warrants further investigation and is explored in this work in chapter 6.

Group V dopants:

With carrier lifetime limited by a tellurium rich stoichiometry, there has recently been a renewed interest in group V doping combined with cadmium rich growth conditions to obtain long lifetimes with high hole density. Phosphorus doped single crystal CdTe has enabled devices with V_{oc} above 1 V due to lifetimes that are near radiatively limited and hole density up to 10^{17} cm^{-3} with a ~50% activation ratio [103]. Arsenic has also been investigated as a potential dopant and shown similar promise [104], although the formation of *AX* centres and secondary phase formation must be carefully controlled [105]. Translating this performance to polycrystalline solar cells has proven challenging due to difficulty in incorporating dopants into the grain interiors, although this can be overcome by incorporating dopants during CdTe deposition [86]. This has enabled efficiencies above 20% with an arsenic doped absorber layer [13]. Antimony has also received renewed interest as a *p*-type dopant for CdTe after the ionisation energy was found to be lower than previously expected. Activation ratios of 19% and ~45% have been achieved in thin films and single crystals respectively, with hole densities in excess of 10^{16} cm^{-3} [86,106]. Figure 3.8 compares phosphorus, arsenic and antimony as *p*-type dopants in CdTe single crystals, which demonstrates the potential of group V doping if similar results can be achieved in thin film solar cells.

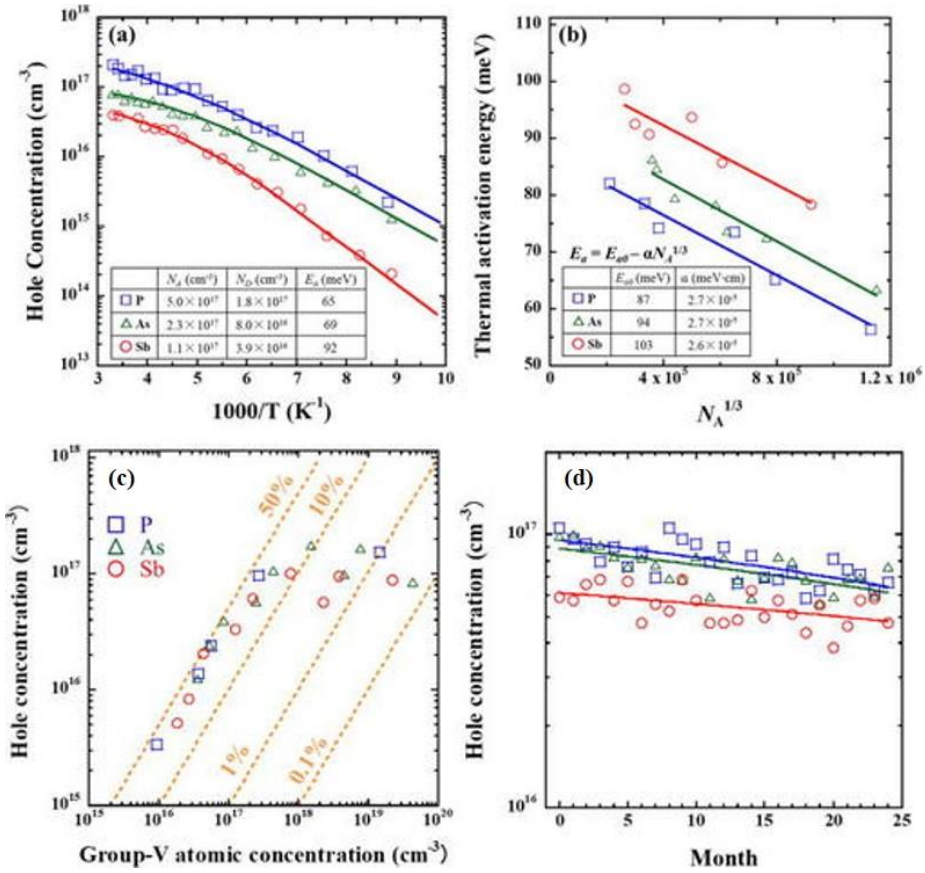

Figure 3.8: A comparison of group V dopants in CdTe single crystals. The (a) hole concentration, (b) activation energy, (c) doping efficiency and (d) stability is compared for samples doped with P, As and Sb, reproduced from ref [106]

3.8 Contacts

CdTe has a relatively deep lying ionisation potential (~ 6 eV) and therefore forming an ohmic contact is challenging. Metals with a work function less than that of CdTe will instead form a Schottky barrier, with an electric field acting in the opposite direction to the main *p-n* junction which limits current in forward bias and causing the commonly observed rollover phenomena (section 2.2.5). The magnitude of such a barrier can be described by the Schottky-Mott rule [107]:

$$\Phi_B = \phi_M - \chi_{SC} \tag{3.1}$$

Since there are no practical metals with a suitably high work function, there inevitably exists a barrier to carrier extraction at the back contact which facilitates recombination and can affect the open circuit voltage and fill factor. A highly defective surface also causes deviations from the Schottky-Mott model whereby barrier height is insensitive to metal work function due to Fermi level pinning, further inhibiting ohmic contacting [108]. Several strategies exist to mitigate the effect of this barrier and therefore form a pseudo-ohmic contact whereby device performance is not limited by a back contact barrier, some of which are outlined below.

3.8.1 Surface treatments

The chlorine activation treatment results in the formation of various oxide and chloride phases at the back surface of CdTe which must be removed prior to contacting. Several pre-contacting treatments have been utilised for this, with chemical etching in a nitric and phosphoric acid mix (NP etch) or a solution of bromine in methanol (Br-MeOH) being most common [109,110]. As well as removing oxide phases, these treatments typically result in a tellurium rich region at the back contact due to preferentially etching Cd. Tellurium has a VBM between that of CdTe and high work function metals, thereby aiding the formation of an ohmic contact by dividing the contact barrier into two smaller ones [111]. However, since these surface treatments preferentially etch defective areas, care must be taken to avoid excessive inhomogeneity and elemental Te accumulation at grain boundaries [112]. Alternatively, a thin layer of tellurium can be deposited at the back surface instead of the removal of cadmium, which is more controllable and does not deplete grain boundaries [113].

3.8.2 p^+ doped surface

A commonly employed strategy to minimise the effect of a contact barrier is to produce a highly p^+ doped region at the back contact which reduces the width of the Schottky barrier, thereby allowing carriers to tunnel across relatively unimpeded [114]. This is often done in

combination with surface etching, combining a tellurium rich surface with an extrinsic dopant to lower the effective barrier height. Although a range of dopants can be used for this purpose, copper is most commonly used to form a Cu_xTe phase whereby the pre-contacting treatment simultaneously lowers the contact barrier height whilst increasing *p*-type doping within the bulk of the absorber layer. As with bulk doping, the use of copper at the back contact can pose stability concerns due to migration along grain boundaries to the front contact [89].

3.8.3 Electron Reflector

A Schottky barrier inhibits carrier extraction by encouraging recombination at the back surface, and therefore an electron reflector can be used to mitigate this. Depositing a semiconductor with an aligned valence band to that of CdTe whilst possessing a larger band gap impedes the transport of electrons towards the depletion region of the back contact. Since recombination requires both carrier types, this lack of electrons can limit back surface recombination. CdMgTe and ZnTe have both been studied extensively for this purpose. Whilst CdMgTe has shown some promise as an electron reflector, magnesium loss during chlorine activation has limited its applicability [115]. With a negligible valence band offset and relative ease of doping, ZnTe has proven successful in aiding the formation of an ohmic contact and has been incorporated into commercial modules [116].

3.8.4 Organic Contacts

Although CdTe solar cells are typically composed entirely of inorganic materials, consideration of organic semiconductors opens an enormous amount of unexplored parameter space as they are highly tuneable which may allow the valence and conduction bands to be optimised for efficient hole extraction and electron reflection. Organic materials can also improve average device performance by reducing the detrimental impact of pinholes by acting as a barrier between the front and back contacts for CdTe [117,118], an approach used in other thin film solar cells [118]. Several polymers such as PEDOT:PSS [119], P3HT [117], PCBM [120], spiro-OMeTAD [121] and polyaniline [118] have been investigated as back contact layers for CdTe solar cells, with P3HT and spiro-OMeTAD in particular showing a beneficial effect. Hybrid organic-inorganic perovskite layers have been employed to systematically tune the valence band position, allowing an increase in efficiency resulting from an improved fill factor and V_{oc} [122]. Alternatively, there have been preliminary reports of using organic layers to create an interfacial dipole to lower the effective barrier height [123]. There are few reports on the use of organic contacts to CdTe and therefore remains enormous scope for further study.

3.8.5 Alternative contacts

There have been a range of other hole transport layers such as Sb_2Te_3, As_2Te_3, MoO_x and many others that facilitate ohmic contacting of CdTe by providing a more easily doped interlayer, high work function or suitable band positions [124–126]. Oxides such as Al_2O_3 have been used to passivate the CdTe back surface, although improving device performance has proven challenging [127]. Whilst back surface recombination has been focus of significant research, it is likely that the full benefits of this only realised after front interface recombination has been improved [128].

3.9 Summary

This chapter describes the development of CdTe-based solar cells from homojunction devices, to the traditional CdS/CdTe heterojunction, and more recent advances towards new device architectures. The key layers in CdTe devices as well as processing options for each stage of cell development are discussed in turn. Following a period of stagnated record efficiency, more transparent window layers combined with a graded absorber layer have recently allowed improved current collection, which has increased the record J_{sc} towards its Shockley-Queisser limit. Strategies to improve V_{oc} beyond historic limits have targeted new doping strategies to achieve a high acceptor concentration with long carrier lifetime, which has been effective in single crystal devices. Translating this to polycrystalline devices has proven challenging, however if successful would allow further increases in the record efficiency and therefore ensure CdTe photovoltaics remains competitive with the more established silicon technologies.

3.10 References

1. Cusano, D. A. The performance of thin film solar cells employing photovoltaic $Cu_{2-x}Te$-CdTe heterojunctions. *Revue de Physique Appliquée* **1**, 195–200 (1966).
2. Adirovich, EI ; Yuabov, YM ; Yagudaev, G. Photoelectric effects in film diodes with CdS-CdTe heterojunctions. *Soviet Physics Semiconductors* **3**, 61–65 (1969).
3. Bonnet, D. & Rabenhorst, H. New results on the development of a thin-film p-CdTe n-CdS heterojunction solar cell. in *Proceedings of the 9th IEEE Photovoltaic Specialists Conference* 129–132 (1972).
4. Wu, X. *et al.* 16.5%-efficient CdS/CdTe polycrystalline thin-film solar cell. in *Proceedings of 17th European Photovoltaic SolarEnergy Conference* 995–1000 (2001).
5. First Solar, Inc. - First Solar Sets World Record for CdTe Solar PV Efficiency [Press Release]. https://investor.firstsolar.com/news/press-release-details/2011/First-Solar-Sets-World-Record-for-CdTe-Solar-PV-Efficiency/default.aspx.
6. Green, M. A. *et al.* Solar cell efficiency tables (version 56). *Progress in Photovoltaics: Research and Applications* **28**, 629–638 (2020).
7. NREL. Best research-cell efficiency chart. www.nrel.gov/pv/cell-efficiency.html (2020).
8. NREL. Champion photovoltaic module efficiency chart. www.nrel.gov/pv/module-efficiency.html (2020).
9. Reese, M. O. *et al.* Increasing markets and decreasing package weight for high-specific-power photovoltaics. *Nature Energy* **3**, 1002–1012 (2018).
10. Kranz, L. *et al.* Doping of polycrystalline CdTe for high-efficiency solar cells on flexible metal foil. *Nature Communications* **4**, 1–7 (2013).
11. Wu, X. High-efficiency polycrystalline CdTe thin-film solar cells. *Solar Energy* **77**, 803–814 (2004).
12. Dhere, R. *et al.* The effect of CdTe deposition temperature on device properties of different TCOs and glass substrates. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 340–344 (2010).
13. Metzger, W. K. *et al.* Exceeding 20% efficiency with in situ group V doping in polycrystalline CdTe solar cells. *Nature Energy* **4**, 837–845 (2019).
14. Durose, K., Edwards, P. R. & Halliday, D. P. Materials aspects of CdTe/CdS solar cells. *Journal of Crystal Growth* **197**, 733–742 (1999).
15. Klenk, R. Characterisation and modelling of chalcopyrite solar cells. *Thin Solid Films* **387**, 135–140 (2001).
16. Song, T., Kanevce, A. & Sites, J. R. Emitter/absorber interface of CdTe solar cells. *Journal of Applied Physics* **119**, 233104 (2016).
17. Birkmire, R. W. & Eser, E. Polycrystalline thin film solar cells: Present status and future potential. *Annual Review of Materials Science* **27**, 625–653 (1997).
18. Gemain, F., Robin, I.-C., Renet, S. & Bernardi, S. Photoluminescence studies of CdS layers for solar cells. *physica status solidi (c)* **9**, 1740–1743 (2012).

19. Burst, J. M. *et al.* Interface characterization of single-crystal CdTe solar cells with V_{OC} > 950 mV. *IEEE Journal of Photovoltaics* **6**, 1650–1653 (2016).

20. Oladeji, I. O., Chow, L., Ferekides, C. S., Viswanathan, V. & Zhao, Z. Metal/CdTe/CdS/$Cd_{1-x}Zn_xS$/TCO/glass: A new CdTe thin film solar cell structure. *Solar Energy Materials and Solar Cells* **61**, 203–211 (2000).

21. Soo, Y. L. *et al.* Local environment surrounding S and Cd in CdS:O thin film photovoltaic materials probed by x-ray absorption fine structures. *Applied Physics Letters* **89**, 131908 (2006).

22. Wu, X. *et al.* Nanostructured CdS:O film: preparation, properties, and application. *physica status solidi (c)* **1**, 1062–1066 (2004).

23. Wei, S. H., Zhang, S. B. & Zunger, A. First-principles calculation of band offsets, optical bowings, and defects in CdS, CdSe, CdTe, and their alloys. *Journal of Applied Physics* **87**, 1304–1311 (2000).

24. Samoilenko, Y., Abbas, A., Michael Walls, J. & Wolden, C. A. Copper-induced recrystallization and interdiffusion of CdTe/ZnTe thin films. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **36**, 031201 (2018).

25. Kephart, J. M., Geisthardt, R. M. & Sampath, W. S. Optimization of CdTe thin-film solar cell efficiency using a sputtered, oxygenated CdS window layer. *Progress in Photovoltaics: Research and Applications* **23**, 1484–1492 (2015).

26. Meysing, D. M. *et al.* Properties of reactively sputtered oxygenated cadmium sulfide (CdS:O) and their impact on CdTe solar cell performance. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **33**, 021203 (2015).

27. Kephart, J. M. *et al.* Band alignment of front contact layers for high-efficiency CdTe solar cells. *Solar Energy Materials and Solar Cells* **157**, 266–275 (2016).

28. Kephart, J. M., Geisthardt, R. M., Ma, Z., McCamy, J. & Sampath, W. S. Reduction of window layer optical losses in CdS/CdTe solar cells using a float-line manufacturable HRT layer. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 1653–1657 (2013).

29. Spalatu, N., Serban, D. & Potlog, T. ZnSe films prepared by the close-spaced sublimation and their influence on ZnSe/CdTe solar cell performance. in *Proceedings of the International Semiconductor Conference, CAS* vol. 2 451–454 (2011).

30. Baines, T. *et al.* Incorporation of CdSe layers into CdTe thin film solar cells. *Solar Energy Materials and Solar Cells* **180**, 196–204 (2018).

31. Das, S. K. & Morris, G. C. Preparation and properties of electrodeposited indium tin oxide/SnO_2/CdTe and indium tin oxide/SnO_2/CdS/CdTe solar cells. *Journal of Applied Physics* **73**, 782–786 (1993).

32. Aranovich, J. A., Golmayo, D., Fahrenbruch, A. L. & Bube, R. H. Photovoltaic properties of ZnO/CdTe heterojunctions prepared by spray pyrolysis. *Journal of Applied Physics* **51**, 4260–4268 (1980).

33. Ablekim, T. *et al.* Tailoring MgZnO/CdSeTe Interfaces for Photovoltaics. *IEEE Journal of Photovoltaics* **9**, 888–892 (2019).

34. Samoilenko, Y., Yeung, G., Zakutayev, A., Reese, M. O. & Wolden, C. A. Combinatorial study of MZO emitters for CdTe-based solar cells. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 2498–2502 (2019).

35. Bittau, F. *et al.* Degradation of Mg-doped zinc oxide buffer layers in thin film CdTe solar cells. *Thin Solid Films* **691**, 137556 (2019).

36. Sanon, G., Rup, R. & Mansingh, A. Band-gap narrowing and band structure in degenerate tin oxide (SnO_2) films. *Physical Review B* **44**, 5672–5680 (1991).

37. Ganose, A. M. & Scanlon, D. O. Band gap and work function tailoring of SnO_2 for improved transparent conducting ability in photovoltaics. *Journal of Materials Chemistry C* **4**, 1467–1475 (2016).

38. Singh, A. K., Janotti, A., Scheffler, M. & Van De Walle, C. G. Sources of electrical conductivity in SnO_2. *Physical Review Letters* **101**, 055502 (2008).

39. Niles, D. W., Rioux, D. & Höchst, H. A photoemission investigation of the SnO_2/CdS interface: A front contact interface study of CdS/CdTe solar cells. *Journal of Applied Physics* **73**, 4586–4590 (1993).

40. Kiliç, Ç. & Zunger, A. N-type doping of oxides by hydrogen. *Applied Physics Letters* **81**, 73–75 (2002).

41. Butler, M. A. Prediction of flatband potentials at semiconductor-electrolyte interfaces from atomic electronegativities. *Journal of The Electrochemical Society* **125**, 228 (1978).

42. Sahm, T., Gurlo, A., Bârsan, N. & Weimar, U. Basics of oxygen and SnO_2 interaction; work function change and conductivity measurements. *Sensors and Actuators, B: Chemical* **118**, 78–83 (2006).

43. Barnes, T. M., Burst, J. M., Reese, M. O. & Perkins, C. L. Semi-insulating Sn-Zr-O: Tunable resistance buffer layers. *Applied Physics Letters* **106**, 092106 (2015).

44. Fuchs, A., Schimper, H. J., Klein, A. & Jaegermann, W. Photoemission studies on undoped SnO_2 buffer layers for CdTe thin film solar cells. in *Energy Procedia* vol. 10 149–154 (2011).

45. Mitchell, K. W. *et al.* Progress towards high efficiency thin film CdTe solar cells. *Solar Cells* **23**, 49–57 (1988).

46. McCandless, B. E. & Dobson, K. D. Processing options for CdTe thin film solar cells. *Solar Energy* **77**, 839–856 (2004).

47. Ablekim, T. *et al.* Thin-film solar cells with 19% efficiency by thermal evaporation of CdSe and CdTe. *ACS Energy Letters* **5**, 892–896 (2020).

48. Luschitz, J., Lakus-Wollny, K., Klein, A. & Jaegermann, W. Growth regimes of CdTe deposited by close-spaced sublimation for application in thin film solar cells. *Thin Solid Films* **515**, 5814–5818 (2007).

49. Burst, J. M. *et al.* CdTe solar cells with open-circuit voltage breaking the 1V barrier. *Nature Energy* **1**, 1–8 (2016).

50. Amarasinghe, M. *et al.* Influence of CdTe deposition temperature and window thickness on CdTe grain size and lifetime after $CdCl_2$ recrystallization. *IEEE Journal of Photovoltaics* **8**, 600–603 (2018).

51. Moseley, J. *et al.* Cathodoluminescence analysis of grain boundaries and grain interiors in thin-film CdTe. *IEEE Journal of Photovoltaics* **4**, 1671–1679 (2014).

52. Li, C. *et al.* Grain-boundary-enhanced carrier collection in CdTe solar cells. *Physical Review Letters* **112**, 156103 (2014).

53. Visoly-Fisher, I., Cohen, S. R. & Cahen, D. Direct evidence for grain-boundary depletion in polycrystalline CdTe from nanoscale-resolved measurements. *Applied Physics Letters* **82**, 556–558 (2003).

54. Visoly-Fisher, I., Cohen, S. R., Gartsman, K., Ruzin, A. & Cahen, D. Understanding the beneficial role of grain boundaries in polycrystalline solar cells from single-grain-boundary scanning probe microscopy. *Advanced Functional Materials* **16**, 649–660 (2006).

55. Visoly-Fisher, I., Cohen, S. R., Ruzin, A. & Cahen, D. How polycrystalline devices can outperform single-crystal ones: Thin film CdTe/CdS solar cells. *Advanced Materials* **16**, 879–883 (2004).

56. Gloeckler, M., Sites, J. R. & Metzger, W. K. Grain-boundary recombination in Cu (In,Ga) Se_2 solar cells. *Journal of Applied Physics* **98**, 113704 (2005).

57. Tong, C. J. & McKenna, K. P. Passivating grain boundaries in polycrystalline CdTe. *Journal of Physical Chemistry C* **123**, 23882–23889 (2019).

58. Fiducia, T. A. M. *et al.* Understanding the role of selenium in defect passivation for highly efficient selenium-alloyed cadmium telluride solar cells. *Nature Energy* **4**, 504–511 (2019).

59. Mao, D., Wickersham, C. E. & Gloeckler, M. Measurement of chlorine concentrations at CdTe grain boundaries. *IEEE Journal of Photovoltaics* **4**, 1655–1658 (2014).

60. Li, C. *et al.* S-Te interdiffusion within grains and grain boundaries in cdte solar cells. *IEEE Journal of Photovoltaics* **4**, 1636–1643 (2014).

61. Moseley, J. *et al.* Recombination by grain-boundary type in CdTe. *Journal of Applied Physics* **118**, 025702 (2015).

62. Green, M. A. Photocurrent loss within the depletion region of polycrystalline solar cells. *Solid State Electronics* **21**, 1139–1144 (1978).

63. Lundberg, O., Edoff, M. & Stolt, L. The effect of Ga-grading in CIGS thin film solar cells. in *Thin Solid Films* vols. 480–481 520–525 (Elsevier, 2005).

64. Swanson, D. E. *et al.* CdCl2 passivation of polycrystalline CdMgTe and CdZnTe absorbers for tandem photovoltaic cells. *Journal of Applied Physics* **123**, 203101 (2018).

65. Munshi, A. H. *et al.* Polycrystalline CdSeTe/CdTe absorber cells with 28 mA/cm^2 short-circuit current. *IEEE Journal of Photovoltaics* **8**, 310–314 (2018).

66. Swanson, D. E., Sites, J. R. & Sampath, W. S. Co-sublimation of $CdSe_xTe_{1-x}$ layers for CdTe solar cells. *Solar Energy Materials and Solar Cells* **159**, 389–394 (2017).

67. Zheng, X. *et al.* Recombination and bandgap engineering in CdSeTe/CdTe solar cells. *APL Materials* **7**, 071112 (2019).

68. Harvey, S. P., Teeter, G., Moutinho, H. & Al-Jassim, M. M. Direct evidence of enhanced chlorine segregation at grain boundaries in polycrystalline CdTe thin films via three-dimensional TOF-SIMS imaging. *Progress in Photovoltaics: Research and Applications* **23**, 838–846 (2015).

69. Wei, S. H. & Zhang, S. B. Chemical trends of defect formation and doping limit in II-VI semiconductors: The case of CdTe. *Physical Review B - Condensed Matter and Materials Physics* **66**, 1–10 (2002).

70. Tai, H. & Hori, S. Equilbirum phase diagrams of the CdTe-$CdCl_2$ and CdTe-$CdBr_2$ systems. *Nippon Kinzoku Gakkaishi/Journal of the Japan Institute of Metals* **40**, 722–725 (1976).

71. Abbas, A. *et al.* The effect of cadmium chloride treatment on close-spaced sublimated cadmium telluride thin-film solar cells. *IEEE Journal of Photovoltaics* **3**, 1361–1366 (2013).

72. Major, J. D., Bowen, L., Treharne, R. & Durose, K. Assessment of photovoltaic junction position using combined focused ion beam and electron beam-induced current analysis of close space sublimation deposited CdTe solar cells. *Progress in Photovoltaics: Research and Applications* **22**, 1096–1104 (2014).

73. Nakayama, N. *et al.* Screen printed thin film CdS/CdTe Solar cell. *Japanese Journal of Applied Physics* **19**, 703–712 (1980).

74. Moon, J. T., Park, K. C. & Im, H. B. Photovoltaic properties of CdS/CdTe solar cells sintered with $CdCl_2$. *Solar Energy Materials* **18**, 53–60 (1988).

75. McCandless, B. E. & Sites, J. R. Cadmium Telluride Solar Cells. in *Handbook of Photovoltaic Science and Engineering* 617–662 (John Wiley & Sons, Ltd, 2005). doi:10.1002/0470014008.ch14.

76. Qu, Y., Meyers, P. V. & McCandless, B. E. HCl vapor post-deposition heat treatment of CdTe/CdS films. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 1013–1016 (IEEE, 1996).

77. Drost, C. *et al.* Activation of CdTe-based thin films with zinc chloride and tetrachlorozincates. in *Thin Solid Films* vol. 582 100–104 (Elsevier, 2015).

78. Mazzamuto, S. *et al.* A study of the CdTe treatment with a Freon gas such as CHF_2Cl. *Thin Solid Films* **516**, 7079–7083 (2008).

79. Major, J. D. *et al.* In-depth analysis of chloride treatments for thin-film CdTe solar cells. *Nature Communications* **7**, 1–10 (2016).

80. Major, J. D., Treharne, R. E., Phillips, L. J. & Durose, K. A low-cost non-toxic post-growth activation step for CdTe solar cells. *Nature* **511**, 334–337 (2014).

81. Kanevce, A., Reese, M. O., Barnes, T. M., Jensen, S. A. & Metzger, W. K. The roles of carrier concentration and interface, bulk, and grain-boundary recombination for 25% efficient CdTe solar cells. *Journal of Applied Physics* **121**, 214506 (2017).

82. Greenberg, J. H. P-T-X phase equilibrium and vapor pressure scanning of non-stoichiometry in CdTe. *Journal of Crystal Growth* **161**, 1–11 (1996).

83. Desnica, U. V. Doping limits in II-VI compounds - Challenges, problems and solutions. *Progress in Crystal Growth and Characterization of Materials* **36**, 291–357 (1998).

84. Ma, J. *et al.* Dependence of the minority-carrier lifetime on the stoichiometry of CdTe using time-resolved photoluminescence and first-principles calculations. *Physical Review Letters* **111**, 067402 (2013).

85. Yang, J.-H., Yin, W.-J., Park, J.-S., Ma, J. & Wei, S.-H. Review on first-principles study of defect properties of CdTe as a solar cell absorber. *Semiconductor Science and Technology* **31**, 083002 (2016).

86. McCandless, B. E. *et al.* Overcoming carrier concentration limits in polycrystalline CdTe thin films with in situ doping. *Scientific Reports* **8**, (2018).

87. Adirovich, E. I., Yuabov, Y. M. & Yagudaev, G. R. Photoelectric effects in film diodes with CdS-CdTe heterojunctions. *Sov Phys Semiconductors* **3**, 61–64 (1969).

88. Perrenoud, J. *et al.* A comprehensive picture of Cu doping in CdTe solar cells. *Journal of Applied Physics* **114**, 174505 (2013).

89. Demtsu, S., Albin, D. & Sites, J. Role of copper in the performance of CdS/CdTe solar cells. in *Conference Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion, WCPEC-4* vol. 1 523–526 (IEEE Computer Society, 2006).

90. Yan, Y., Jones, K., Zhou, J., Wu, X. & Al-Jassim, M. TEM study of locations of Cu in CdTe solar cells. in *Materials Research Society Symposium Proceedings* vol. 1012 241–246 (Cambridge University Press, 2007).

91. Dobson, K. D., Visoly-Fisher, I., Hodes, G. & Cahen, D. Stability of CdTe/CdS thin-film solar cells. *Solar Energy Materials and Solar Cells* **62**, 295–325 (2000).

92. Kučys, E., Jerhot, J., Bertulis, K. & Bariss, V. Copper impurity behaviour in CdTe films. *Physica Status Solidi (a)* **59**, 91–99 (1980).

93. Capper, P. *Properties of narrow gap cadmium-based compounds*. (Institution of Engineering and Technology, 1994). doi:10.1016/0961-1290(95)80115-4.

94. Chamonal, J. P., Molva, E., Pautrat, J. L. & Revoil, L. Complex behaviour of Ag in CdTe. *Journal of Crystal Growth* **59**, 297–300 (1982).

95. Emziane, M., Durose, K., Halliday, D. P., Romeo, N. & Bosio, A. SIMS depth profiling of CdTe-based solar cells grown on sapphire substrates. *Thin Solid Films* **511–512**, 66–70 (2006).

96. Crowder, B. L. & Hammer, W. N. Shallow acceptor states in ZnTe and CdTe. *Phys. Rev.* **150**, 541–545 (1966).

97. Duenow, J. N. *et al.* Single-crystal CdTe solar cells with V_{oc} greater than 900 mV. *Applied Physics Letters* **105**, 053903 (2014).

98. Kranz, L. *et al.* Effect of sodium on recrystallization and photovoltaic properties of CdTe solar cells. *Solar Energy Materials and Solar Cells* **105**, 213–219 (2012).

99. Durose, K. *et al.* The influence of NaCl on the microstructure of CdS films and CdTe solar cells. in *Microscopy of Semiconductor Materials* 207–210 (1999).

100. Amirkhalili, A., Barrioz, V., Irvine, S. J. C., Beattie, N. S. & Zoppi, G. A combined Na and Cl treatment to promote grain growth in MOCVD grown CdTe thin films. *Journal of Alloys and Compounds* **699**, 969–975 (2017).

101. Dhere, R. *et al.* Effect of Na incorporation on the growth and properties of CdTe/CdS devices. in *Conference Record of the Thirty-first IEEE* 279–282 (IEEE, 2005).

102. Kurley, J. M. *et al.* Transparent ohmic contacts for solution-processed, ultrathin CdTe solar cells. *ACS Energy Letters* **2**, 270–278 (2017).

103. Burst, J. M. *et al.* CdTe solar cells with open-circuit voltage breaking the 1V barrier. *Nature Energy* **1**, 1–8 (2016).

104. Nagaoka, A., Kuciauskas, D., McCoy, J. & Scarpulla, M. A. High p-type doping, mobility, and photocarrier lifetime in arsenic-doped CdTe single crystals. *Applied Physics Letters* **112**, 192101 (2018).

105. Ablekim, T. *et al.* Self-compensation in arsenic doping of CdTe. *Scientific Reports* **7**, 1–9 (2017).

106. Nagaoka, A. *et al.* Comparison of Sb, As, and P doping in Cd-rich CdTe single crystals: Doping properties, persistent photoconductivity, and long-term stability. *Applied Physics Letters* **116**, 132102 (2020).

107. Tyagi, M. S. Physics of Schottky Barrier Junctions. in *Metal-Semiconductor Schottky Barrier Junctions and Their Applications* 1–60 (Springer US, 1984). doi:10.1007/978-1-4684-4655-5_1.

108. Bardeen, J. Surface states and rectification at a metal semi-conductor contact. *Physical Review* **71**, 717–727 (1947).

109. Sarlund, J., Ritala, M., Leskelä, M., Siponmaa, E. & Zilliacus, R. Characterization of etching procedure in preparation of CdTe solar cells. *Solar Energy Materials and Solar Cells* **44**, 177–190 (1996).

110. Kotina, I. M. *et al.* Study of CdTe etching process in alcoholic solutions of bromine. *Semicond. Sci. Technol* **13**, 890–894 (1998).

111. Song, T., Moore, A. & Sites, J. R. Te layer to reduce the CdTe back-contact barrier. *IEEE Journal of Photovoltaics* **8**, 293–298 (2018).

112. Misra, S. *et al.* Cadmium selective etching in CdTe solar cells produces detrimental narrow-gap Te in grain boundaries. *ACS Applied Energy Materials* **3**, 1749–1758 (2020).

113. Moffett, C. E. & Sampath, W. S. Characterization of tellurium as a back contact for CdTe solar cells. in *2017 IEEE 44th Photovoltaic Specialist Conference (PVSC)* 2736–2739 (2017).

114. Fahrenbruch, A. L. Ohmic contacts and doping of CdTe. *Solar Cells* **21**, 399–412 (1987).

115. Swanson, D. E. *et al.* $CdCl_2$ passivation of polycrystalline CdMgTe and CdZnTe absorbers for tandem photovoltaic cells. *Journal of Applied Physics* **123**, 203101 (2018).

116. Gessert, T. A. *et al.* Development of Cu-doped ZnTe as a back-contact interface layer for thin-film CdS/CdTe solar cells. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **14**, 806–812 (1996).

117. Major, J. D. *et al.* P3HT as a pinhole blocking back contact for CdTe thin film solar cells. (2017) doi:10.1016/j.solmat.2017.07.005.

118. Roussillon, Y., Giolando, D. M., Shvydka, D., Compaan, A. D. & Karpov, V. G. Blocking thin-film nonuniformities: Photovoltaic self-healing. *Appl. Phys. Lett* **84**, (2004).

119. Wang, W., Paudel, N. R., Yan, Y., Duarte, F. & Mount, M. PEDOT:PSS as back contact for CdTe solar cells and the effect of PEDOT:PSS conductivity on device performance. *Journal of Materials Science: Materials in Electronics* **27**, 1057–1061 (2016).

120. Walkons, C., Guralnick, B., McCandless, B. & Birkmire, R. CdTe solar cells with a PCBM back contact. in *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)* 1567–1572 (IEEE, 2014).

121. Du, X. *et al.* Improvement in open-circuit voltage of thin film solar cCells from aqueous nanocrystals by interface engineering. *ACS Applied Materials & Interfaces* **8**, 900–907 (2016).

122. Bhandari, K. P. *et al.* Applications of hybrid organic-inorganic metal halide perovskite thin film as a hole transport layer in CdTe thin film solar cells. in *2017 IEEE 44th Photovoltaic Specialist Conference (PVSC)* 748–751 (2017).

123. Ferekides, C. S. & Morel, D. L. Process Development for High Voc CdTe Solar Cells. Related Information: Work performed by University of South Florida, Tampa, Florida (2011) doi:10.2172/1016430.

124. Paudel, N. R., Xiao, C. & Yan, Y. CdS/CdTe thin-film solar cells with Cu-free transition metal oxide/Au back contacts. *Progress in Photovoltaics: Research and Applications* **23**, 437–442 (2015).

125. Romeo, N., Bosio, A., Mazzamuto, S., Romeo, A. & Vaillant-Roca, L. High efficiency CdTe/CdS thin film solar cells with a novel back contact. *22nd European Photovoltaic Solar Energy Conference* 20–22 (2007).

126. Romeo, N., Bosio, A., Tedeschi, R., Romeo, A. & Canevari, V. A highly effcient and stable CdTe/CdS thin film solar cell. *Solar Energy Materials & Solar Cells* **58**, 209–218 (1999).

127. Danielson, A. *et al.* Sputtered aluminum oxide and p+ amorphous silicon back-contact for improved hole extraction in polycrystalline CdSexTe1-x and CdTe photovoltaics. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 3018–3023 (Institute of Electrical and Electronics Engineers Inc., 2019).

128. Duenow, J. N. & Metzger, W. K. Back-surface recombination, electron reflectors, and paths to 28% efficiency for thin-film photovoltaics: A CdTe case study. *Journal of Applied Physics* **125**, 053101 (2019).

Chapter 4

Experimental Methods

4.1 Introduction

This chapter outlines the working principle of the experimental techniques employed throughout this work to grow and characterise semiconductor thin films as well as complete solar cells. This is presented in three sections. A range of deposition technologies are described in section 4.2 together with key parameters that can be varied to control film properties, as well as the device processing steps required to make complete solar cells. This is followed by section 4.3 which outlines a range of techniques used to characterise the structural, optical and electronic properties of individual films. Finally, section 4.4 describes how key properties of complete solar cells are measured to evaluate device performance.

4.2 Thin film growth and device fabrication

This section describes the working principle of several deposition methods used to the individual layers required for solar cell fabrication, as well as post deposition processing steps required to achieve high performance. Whilst typical conditions are briefly mentioned for each method, further details on the exact experimental procedures used in this work are given in the device fabrication section of the relevant results chapters.

4.2.1 Close Space Sublimation

Close spaced sublimation (CSS) is a common physical vapour deposition method used for depositing thin films of materials with high melting point. Fast deposition rates with a range of adjustable control parameters make it a highly scalable option for high throughput solar cell manufacturing. In contrast to evaporation, the material to be deposited sublimes thereby transitioning directly from a solid to gas phase, which is achieved by heating a source material under a backfilled pressure of a non-reactive gas such as N_2 or Ar. This allows for thin film deposition to be carried out at higher substrate temperatures than achievable for evaporation, since re-sublimation from the substrate is discouraged at higher pressure. This is especially important for the growth of CdTe solar cells whereby performance is often correlated with deposition temperature [1]. The relatively low vapour density of sublimated material produced by CSS necessitates the close proximity of the source and substrate, which are typically separated by a few millimetres, although closely related variants of this technique such as vapour transport deposition can overcome this by spatially separating the sublimation and deposition processes.

CdTe is particularly suited to CSS deposition since it sublimes congruently, reversibly dissociating into its component elemental vapours which are transferred to the surface of the substrate by a temperature gradient where they recombine to form a thin film. Deposition is typically carried out with substrate and source temperatures of around 500 °C and 600 °C respectively with a chamber pressure of 10 – 30 Torr N_2 allowing suitable growth rates.

$$2\,CdTe_{\,(s)} \rightleftharpoons 2\,Cd_{\,(g)} + Te_{2\,(g)} \tag{4.1}$$

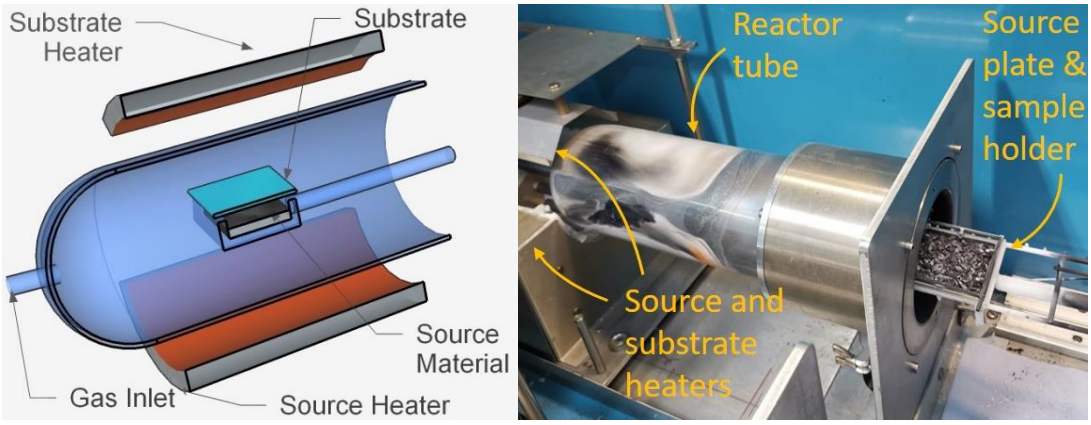

Figure 4.1: Schematic diagram (a) and photograph (b) of the of the CSS deposition chamber used in this work to grow CdTe, which is custom built by Electro-Gas Systems Ltd.

The CSS deposition system used in this work was custom built by Electro-Gas Systems Ltd, with a schematic diagram as well as photograph of the CdTe growth chamber shown in Figure 4.1. The growth chamber is composed entirely of high purity quartz to avoid possible film contamination and a vacuum is maintained using a scroll pump. The gas ambient is controlled by an automatic pressure controller, with mass flow controllers used to alter the N_2/O_2 or N_2/H_2 partial pressure. A tungsten coil heater is placed below the chamber to heat the source tray, which is filled with 5N purity CdTe polycrystalline lumps (Alfa Aesar) and monitored with a thermocouple and PID temperature controller. Independent temperature control of the substrate is possible using an infrared ceramic heater, although this is not normally necessary due to the proximity of the source and substrate, with thermal coupling resulting in a ~100°C temperature difference at standard deposition temperatures. Growth duration is usually controlled by nitrogen pressure, with 400 Torr preventing appreciable deposition over typical processing timescales and thereby acting as a gas "shutter" to terminate growth. Where more precision is required, a physical shutter can also be inserted between the source and the substrate the start and stop deposition more controllably.

4.2.2 Thermal Evaporation

Thermal evaporation is achieved by resistively heating a source material within a moderate vacuum. This increases the vapour pressure such that material travels in a straight line with few collisions with residual gas atoms, thereby allowing a reasonable deposition rate after condensing onto a substrate. Figure 4.2 shows the main components of the thermal evaporation systems used whereby a current is passed through a filament to resistively heat a boat containing the source material to be deposited. Evaporation is initiated by removal of a shutter and monitored in-situ with a quartz crystal microbalance. A rotating substrate improves film uniformity, whilst the substrate temperature can be controlled to alter growth kinetics. A more detailed description of the principles behind vacuum evaporation is given in ref [2].

Two thermal evaporation systems were used within this work: a Moorfield 307 for deposition of NaF layers at a rate of ~0.2 Å/s and an Oerlikon UNIVEX 300 for Au deposition at a rate of ~10 Å/s. Both systems have a typical base pressure $<10^{-5}$ Torr. The substrate was rotated for NaF deposition but stationary for Au deposition, with no substrate heating in either case.

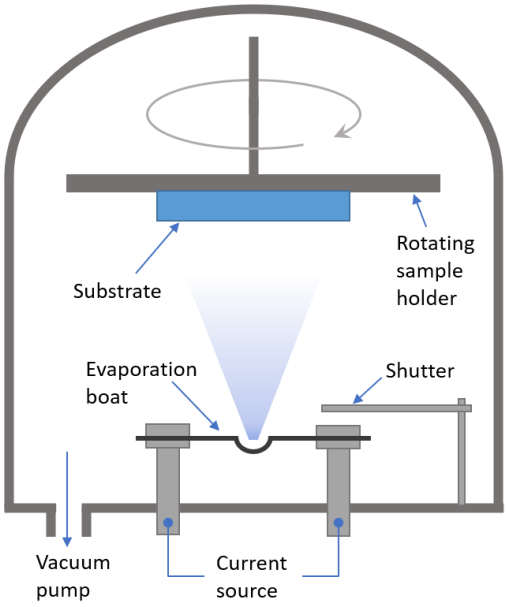

Figure 4.2: Schematic diagram showing the main components of a typical thermal evaporation chamber representative of those used within this work.

4.2.3 Sputter Deposition

Sputtering occurs where a target material is bombarded by energetic atoms (typically ions accelerated by an electric field) with the resulting momentum transfer releasing particles from the surface. When these ejected particles are directed towards a substrate, film growth proceeds via sputter deposition. In its simplest implementation, diode sputtering, deposition occurs when free electrons are accelerated away from a cathode by a static electric field, ionising gas atoms which are then accelerated towards the cathode, releasing sputtered atoms towards the substrate. Magnetron sputtering increases the plasma density near to the cathode by introducing permanent magnets below the target to trap electrons, thereby increasing the likelihood of collisions and therefore increasing the deposition rate significantly. By replacing the DC bias voltage with an alternating RF voltage, charge build up on the surface of the target is prevented as neutrality is restored every half cycle which allows deposition of non-conducting materials, albeit at a slower rate. Deposition typically occurs in an inert gas atmosphere such as Ar, with chamber pressure < 10 mTorr. Compounds can be deposited by sputtering directly from a target, or by sputtering from an elemental target in the presence of a partial pressure of a reactive gas such as nitrogen or oxygen. Further details of sputter deposition can be found in ref [3,4].

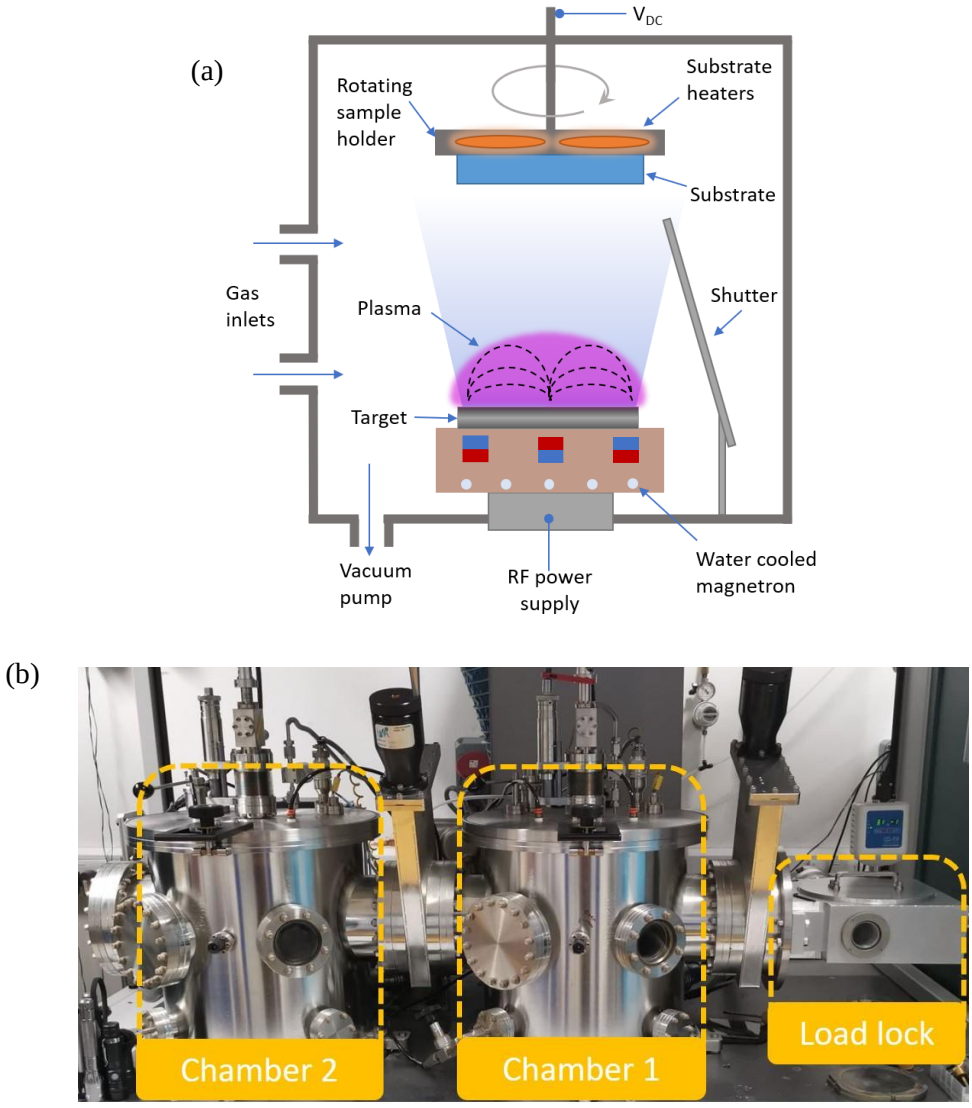

Figure 4.3: (a) Schematic diagram showing the main components of an RF magnetron sputtering system, and (b) photograph of the AJA Orion 8 dual chamber system used in this work.

Radio frequency magnetron sputtering is used in this work to deposit thin films of CdS, CdSe and CdTe in an AJA Orion 8 deposition system, shown in Figure 4.3. This has two linked deposition chambers, and each chamber can simultaneously house up to five targets in a confocal sputter-up configuration. Substrate temperature is controlled by halogen lamps behind the sample holder connected to a PID controller. A constant flow of 20 sccm Ar is introduced into the chamber and pressure is controlled by an automated throttle gate valve. An RF supply is connected to each target, delivering 60 – 150 W to each 3" diameter target. The substrate temperature, growth pressure and RF power comprise the key deposition parameters, allowing growth time calibrated ex-situ using surface profilometry.

4.2.4 Spin Coating

Spin coating is a simple and inexpensive solution processing technique commonly used to deposit nanoparticles and organic semiconductor layers. The material to be deposited is dissolved in a volatile solvent and the resulting solution is dropped onto either a stationary (static dispense) or rotating (dynamic dispense) substrate. The solution is then spread across the substrate by spinning it at high speed (~1000 – 6000 rpm), whereby the majority is thrown over the edge by centrifugal force whilst the remaining solvent evaporates leaving a uniform film with thickness inversely proportional to the square root of the substrate angular velocity.

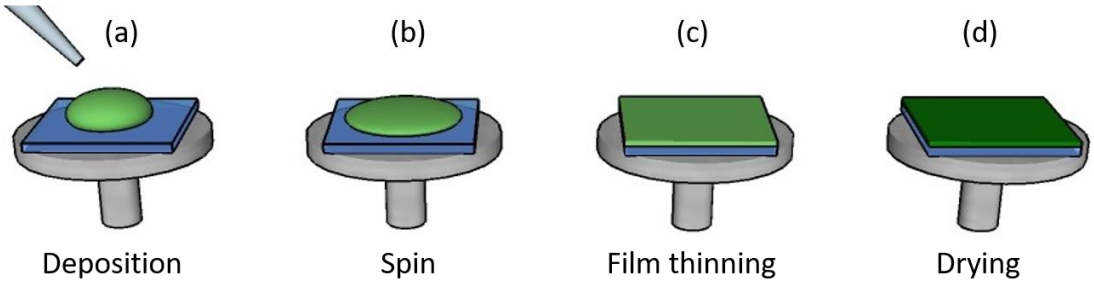

Figure 4.4: Diagram showing the main steps involved during spin coating: (a) a solution is dropped from a pipette onto the centre of a substrate, (b) the substrate is brought to the desired rotation speed, spreading the solution outwards, (c) as the solution is flung off the edge of the substrate the film becomes thinner and more viscous, and (d) the remaining solvent is evaporated, leaving behind a uniform thin film of the desired material.

Figure 4.4 shows the main steps involved in the spin coating process. This process may be carried out in one or more stages at different rotational speed and acceleration. Film properties are also influenced by the solution concentration, choice of solvent and the ambient conditions under which the film dries. A Laurell 650 series spin coater was used in this work with dynamic spin coating to ensure uniformity and prevent early solvent evaporation.

4.2.5 Post growth chlorine activation treatment and etching

Film stacks with as-deposited CdTe layers result in poor device performance and require chlorine activation treatment to produce high efficiency solar cells (section 3.6). Devices in this work were treated using $MgCl_2$, rather than the more conventional $CdCl_2$, due to its low toxicity and therefore ease of processing. A 1M solution of $MgCl_2$ in H_2O (Alfa Aesar) was deposited onto the back surface of CdTe films via spray coating, before samples were annealed in a tube furnace for 20 min. Activation temperatures were between 410°C – 430°C, and were carried out in an air ambient.

To remove oxides and create a Te rich surface, CdTe films were etched in a dilute nitric-phosphoric (NP) acid (H_2O : HNO_3: H_3PO_4 in a 29 : 1 : 70 ratio). Samples were submerged in this etchant for 15 seconds both before and after chlorine activation, before rinsing with de-ionised water and dried with nitrogen.

4.3 Thin film characterisation

This section describes the theory underpinning a range of measurement techniques used to characterise individual thin films over the course of this work.

4.3.1 Profilometry

Film thickness was measured using an AMBIOS XP-200 surface profiler to calibrate several deposition processes. To achieve this a small section of the film is removed by mechanical scribing, etching, or masking part of the substrate prior to deposition. A stylus is then brought into contact with the surface with a specified force and a line is scanned across the edge of the step between the film and the exposed substrate. The change in height of the stylus is measured as it is scanned across the sample, thereby allowing the height of the film to be determined.

4.3.2 Scanning Electron Microscopy

Scanning electron microscopy allows samples to be imaged at high resolution by raster scanning an electron beam focused on the surface of a sample as shown in Figure 4.5a. The beam is accelerated towards an anode and directed by a series of electromagnetic lenses, over the surface of a sample. The interaction of these electrons with a surface generates several signals such as secondary electrons, backscattered electrons, x-rays and other photons which can be collected by dedicated detectors for analysis. The electron beam which probes the sample interacts within a characteristic generation volume depending on the accelerating voltage, spot size and material parameters as shown in Figure 4.5b. Each of the signals collected during a measurement are produced preferentially in a specific area within the generation volume and can offer complementary information. Secondary electrons are generated close to the sample surface via inelastic scattering and the roughness of a surface and placement of the detector creates a shadowing effect which allows imaging with topographical contrast. Backscattered electrons are elastically scattered deeper within the sample and are sensitive to atomic weight, therefore this imaging mode provides elemental contrast. Energy dispersive x-ray detectors (EDX) are often attached to electron microscopes to detect characteristic x-rays produced by the inelastic interaction of electrons within a sample. This technique can be used to provide quantitative information on the spatial distribution of elements within a sample.

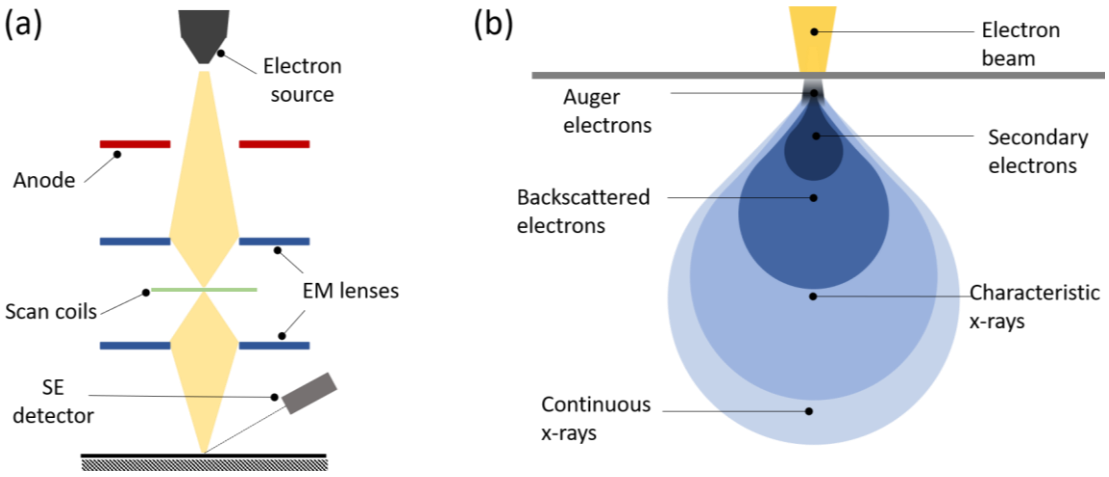

Figure 4.5: Diagrams showing (a) the main components of a typical scanning electron microscope and (b) the interaction volume of an electron beam within a sample surface showing the generation depth from which various SEM signals originate

Two microscopes were used in this work: a JEOL JSM-7001F (ICaL, University of Liverpool), which is equipped with an Oxford instruments INCA X-act EDX detector, and Hitachi SU70 (GJ Russell Electron Microscope Facility, Durham University). Secondary electron imaging and EDX measurements were performed with typical accelerating voltage between 5 – 20 kV.

4.3.3 Focused Ion Beam

A focused ion beam (FIB) can be used to image samples in a similar manner to SEM imaging. Both operate on similar principles, however a FIB utilises a focused, low energy ion beam in place of an electron beam to excite secondary electrons or ions which are subsequently captured for imaging. Higher beam energies can be used to intentionally remove atoms from the surface of the sample and therefore precisely cut through layers of a samples, which is typically used to prepare samples for subsequent analysis.

A FEI Helios NanoLab 600 Dual Beam system was used in this work, with a liquid metal ion source producing a beam of Ga^+ ions to prepare samples for SEM imaging. This allows the cross section of devices to be accessed by performing a series of FIB cuts and imaging the newly exposed surface.

4.3.4 X-ray Diffraction

The scattering of photons by the electron density surrounding regularly spaced atoms in a crystal gives rise to diffraction of x-rays of wavelength close to the interatomic distance. X-ray diffraction (XRD) measurements rely on the constructive and destructive interference of diffracted x-rays such that crystallographic planes can be identified by observing where in-phase photons satisfy Bragg's Law, which relates the angle of diffraction (θ) to the interplanar distance (d_{hkl}):

$$n\lambda = 2\, d_{hkl} \sin\theta \tag{4.2}$$

Where λ is the wavelength of the incoming photons and n is the order of diffraction. The diffracted intensity is maximised where Bragg's Law is satisfied and is reduced elsewhere. By focussing a monochromatic x-ray beam towards a sample at angle θ and measuring the diffracted intensity at 2θ, a diffractogram can be plotted with peaks corresponding to the hkl planes within the crystal. For a cubic crystal, the lattice constant (a) is related to the plane spacing for a given hkl direction (d_{hkl}) by:

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \tag{4.3}$$

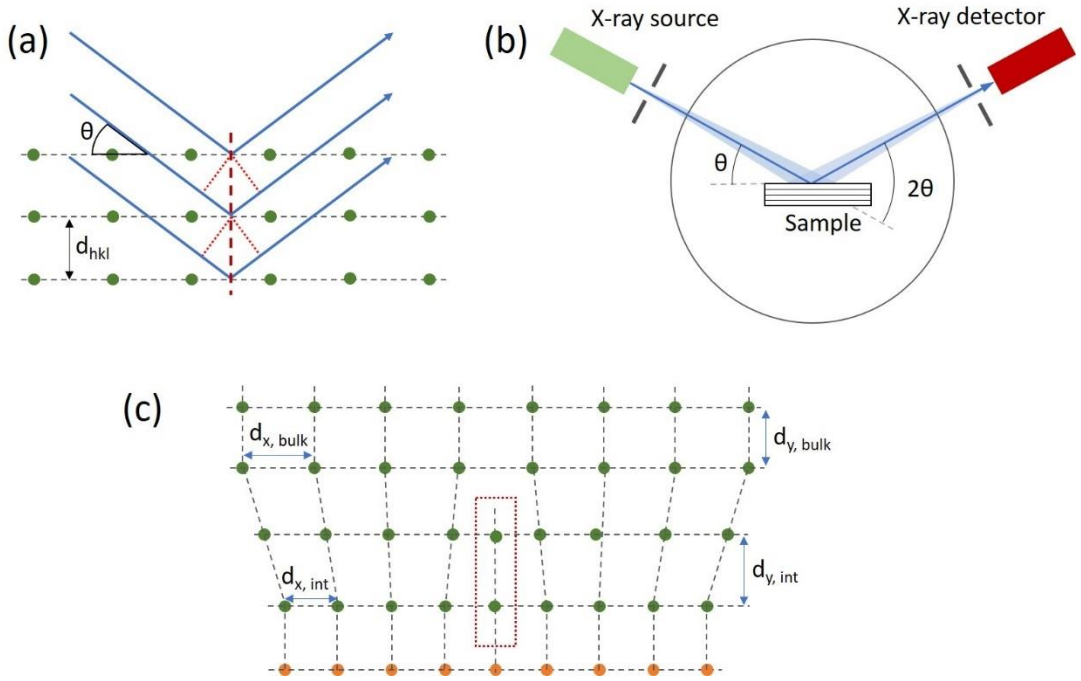

Figure 4.6: (a) Diffraction of x-rays from a certain hkl crystal plane demonstrating the difference in path length producing the interference effects underpinning Bragg's Law, (b) diagram showing a typical diffractometer setup for a $\theta - 2\theta$ scan, and (c) diagram showing lattice distortion caused by film growth (green circles) on a lattice mismatched substrate (orange circles), with an example of a misfit dislocation needed to accommodate the strain highlighted in red

A highly ordered crystalline sample will produce sharp, well defined diffraction peaks in a diffractogram, however there can be several reasons why this may not be the case in practice. Peak broadening is ever present to some extent due to the resolution of the instrument on which measurements are carried out, as well as contributions from the sample due to imperfections in the crystal lattice. Variation in peak width between samples can arise due to changes in the lattice plane spacing:

- Changes in the composition of a material, for example due to alloying, will alter the lattice spacing and cause a shift in the peak position according to Bragg's law (i.e. equation (4.2)). A non-uniform composition within a sample volume will result in a broad diffraction peak due to contributions from a varying lattice constant.

- Inhomogeneous strain, such as that shown in Figure 4.6c, can result when a film is grown atop a substrate with a dissimilar lattice constant. In this case, the lattice constant at the interface will differ from that in the bulk to match that of the substrate. In-plane compressive strain at the interface will result in out-of-plane tensile strain, with lattice spacing varying according to Poisson's ratio, which is gradually relaxed away from the interface. This variation in lattice constant as a function of distance from the interface can therefore cause peak broadening in XRD measurements.

For a thin film, the diffraction pattern produced can be compared to that expected for a randomly oriented powder sample of the same material to determine the texture coefficient, which shows the extent to which a preferential growth along a particular orientation exists within a sample. The texture coefficient (C_{hkl}) of a set of hkl planes can be calculated using the Harris method [5]:

$$C_{hkl} = \frac{I_{hkl}}{I_{0,hkl}} \times \frac{N}{\sum\left(\frac{I_{hkl}}{I_{0,hkl}}\right)} \tag{4.4}$$

Where I_{hkl} and $I_{0,hkl}$ are the diffraction intensities of a specific peak from the measured sample and that expected for a randomly oriented powder sample respectively, and N is the total number of peaks considered. The standard deviation (σ) of the texture coefficient of all considered peaks then gives an indication of the overall level of preferred orientation, with higher values representing a more highly oriented sample:

$$\sigma = \sqrt{\sum \frac{1}{N}(C_{hkl} - 1)^2} \tag{4.5}$$

A Rigaku SmartLab diffractometer was used in this work in parallel beam configuration, utilising a rotating Cu x-ray source with a Ge(220) monochromator to deliver Kα (1.5406 Å) radiation and HyPix-3000 detector in 1D mode.

4.3.5 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) is a highly sensitive, destructive technique which measures the composition of a sample with detection limits in the ppm – ppb range. A primary ion beam is used to sputter the surface of a sample and the ejected ions are identified in a mass spectrometer. Dynamic SIMS continuously bombards the sample which causes the surface to be gradually eroded, thereby producing a depth profile of the elemental distribution. Time of flight SIMS (ToF-SIMS) replaces the standard mass spectrometer with a time-of-flight tube which allows different ionic species to be measured simultaneously and is generally more surface sensitive since a low fluence primary ion beam is typically used which results in a low sputtering rate. Depth profiling is possible by repeatedly switching to a secondary sputter source to produce ions from throughout the depth of a sample.

Two instruments were used in this work: a Hiden Analytical gas ion gun and quadrupole detector with a 5 keV oxygen primary beam was used for dynamic SIMS measurements (Northumbria University) as well as an ION-TOF ToF SIMS V instrument (Imperial College London) with a 25 keV Bi primary ion beam, and O_2 sputter beam used for depth profiling. Concentrations of the elemental distributions in the CdTe layer shown in chapter 7 were quantified by comparing the measured intensities to ion implanted samples of CdTe processed under identical conditions (Surrey Ion Beam Centre). These quantitative elemental concentrations are calibrated for the CdTe layer only. Analysis in other layers of the solar cell can have a degree of variation due to matrix effects whereby the probability of sputtering varies according to an atom's local environment.

4.3.6 X-ray Photoemission Spectroscopy

X-ray photoemission spectroscopy (XPS) is a surface sensitive technique which probes the electronic structure of material by measuring the kinetic energy of electrons released from a sample irradiated with monochromatic x-rays. The transfer of energy from photons with known energy to electrons within the sample causes some of these electrons to gain enough energy to be released into the vacuum via the photoelectric effect. Assuming no energy is lost during photoemission, the kinetic energy (E_k) of the emitted electrons is therefore dependent upon the incoming photon energy ($h\nu$), work function of the analyser (ϕ_A) and binding energy of the photoelectrons (E_B).

$$E_B = h\nu - E_k - \phi_A \tag{4.6}$$

The binding energy can then give information on the chemical environment of photoelectrons which are emitted from populated energy levels. The short inelastic mean free path of electrons

in materials means that XPS is highly surface sensitive, probing up to ~5 nm into the sample. Further details on the operating principle of XPS measurements can be found in ref [6].

In this work, samples were mounted to a sample plate with tantalum straps and placed inside an ultra-high vacuum chamber with base pressure of ~10^{-10} mbar. Core level and valence band measurements were taken using an Al Kα x-ray source (1486.6 eV) operating at 200 W and a Scienta SE200 hemispherical electron energy analyser.

4.3.7 Time Resolved Photoluminescence

Electrons in a material can be excited to higher energy states upon absorption of monochromatic photons of sufficient energy. Photoluminescence (PL) describes the emission of photons released as these electrons revert to their lower energy state, with the photon energy corresponding to a specific radiative transition. The average time an electron resides in an excited state can give information on the material quality, with defects aiding non-radiative recombination processes and therefore decreasing the average carrier lifetime. Time resolved photoluminescence (TRPL) gives an indication of the average lifetime by measuring the total photoluminescence intensity decay rate following excitation from a laser pulse. The decay in PL intensity is the result of both radiative (τ_{rad}), Auger (τ_{Aug}) and defect mediated (τ_{SRH}) contributions from recombination processes that occur within the bulk (τ_{bulk}), as well as a surface lifetime ($\tau_{surface}$). This leads to an overall effective lifetime (τ_{eff}) given by [7]:

$$\frac{1}{\tau_{eff}} = \left(\frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}}\right) + \frac{1}{\tau_{surface}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \qquad (4.7)$$

For materials with a large absorption coefficient and high surface recombination velocity (such as CdTe), the effective lifetime is typically dominated by a small $\tau_{surface}$. A passivated surface is therefore required to obtain information relating to the bulk material. For CdTe solar cells, this is typically achieved by illuminating the sample from the glass side, which results in absorption away from the exposed back surface and close to the junction region instead. Typical TRPL measurements taken from the front and back surface of CdTe samples are shown in Figure 4.7.

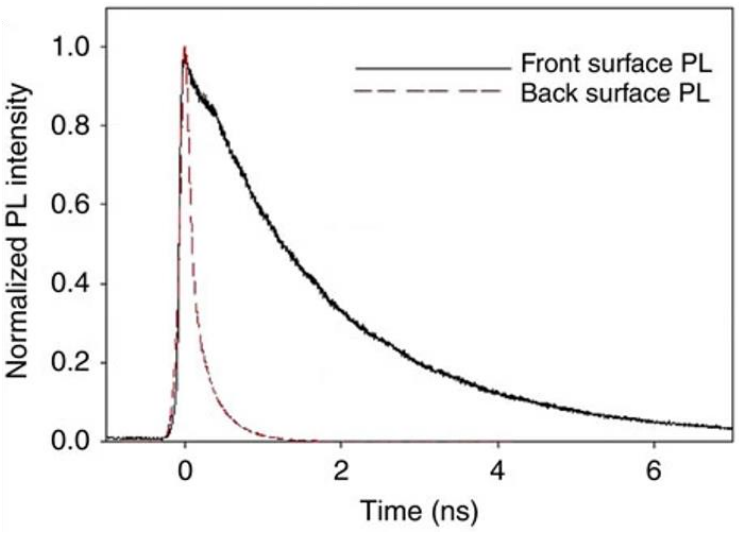

Figure 4.7: Example of TRPL measurement taken from the front (glass side) and back (absorber side) surface of CdTe solar cells, reproduced from ref [8].

TRPL measurements of CdTe typically display a bi-exponential decay in PL intensity (I), as seen for the front surface PL excitation in Figure 4.7. The short lifetime component τ_1 is normally related to charge separation effects (i.e. drift/diffusion) and the longer lifetime component τ_2 is used to track the minority carrier lifetime, with respective amplitudes A_1 and A_2 as shown in equation (4.8). However, care is needed in the interpretation of TRPL measurements to avoid experimental conditions where charge separation effects dominate to ensure accurate determination of the minority carrier lifetime [9].

$$I = A_1 \exp\left(-\frac{t}{\tau_1}\right) + A_2 \exp\left(-\frac{t}{\tau_2}\right) \tag{4.8}$$

A Horiba Jobin Yvon spectrometer was used in this work for TRPL measurements taken at Northumbria University with a 1200 grooves/mm diffraction grating using pulsed laser diode excitation directed towards the glass side of the device at 650 nm and a repetition rate of 25 MHz.

4.3.8 Spectrophotometry

Transmission (T) and reflectance (R) measurements were taken using monochromatic light directed towards thin film samples and appropriately placed detectors. By measuring a film's thickness (d) via profilometry (section 4.3.1), the absorption coefficient (α) can then be calculated [10]:

$$\alpha = \frac{1}{d} \ln\left(\frac{1 - R^2}{T}\right) \tag{4.9}$$

The Tauc method [11] can then be used to determine the optical band gap of samples by plotting $(\alpha hv)^n - hv$ and extrapolating the linear region indicating the absorption edge to the x-axis, where $n = 2$ for direct transitions and $n = 1/2$ for indirect transitions. An example of band gap determination via the Tauc method is shown below in Figure 4.8 for a direct band gap semiconductor.

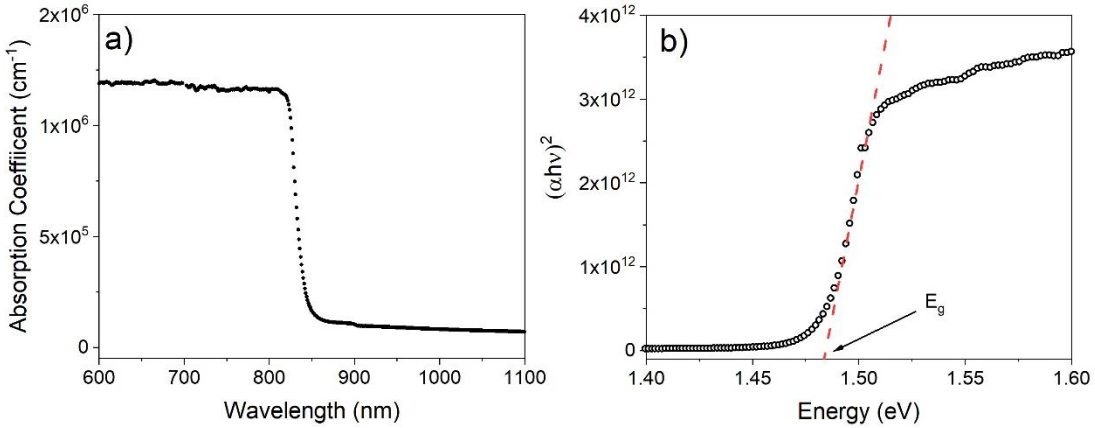

Figure 4.8: (a) Example of absorption coefficient as a function of wavelength, determined from transmission and reflectance measurements and calculated using equation (4.9), and (b) the corresponding Tauc plot where $n = 2$, demonstrating how the band gap is determined by extrapolation of the linear region towards the abscissa

Measurements were taken using a Shimadzu SolidSpec-3700 UV-vis spectrophotometer with readings taken at 2 nm intervals between wavelengths of 500 – 1500 nm. This instrument was also used to estimate the fractional pinhole area of CdTe films by averaging the above band gap light transmission between 500 – 800 nm.

4.4 Solar cell characterisation

4.4.1 Current density – Voltage

Current density – voltage (*JV*) measurements were taken at room temperature using a Keithley 2400 source measure unit, connected to a computer via GPIB interface and controlled using a custom LabView program. Current output was measured at 101 bias points between -1 V to + 1 V for each scan. Where measurements were taken under illumination, a TS Space Systems solar simulator (class AAA) was calibrated to 1000 W/m^2 using a GaAs reference device, which has a band gap well matched to that of CdTe. Analysis of the measured *JV* curves allowed the performance parameters of a device to be determined as described in section 2.4.1. Series and shunt resistances were determined from the gradient of *JV* curves close to V_{oc} and J_{sc} respectively.

4.4.2 Current density – Voltage – Temperature

Current density – voltage measurements were taken as a function of temperature (*JVT*) in the dark using a Keithley SMU and LabView software as described previously, whilst the sample remained in contact with the cold finger of a Janis CCS-450 cryostat. The sample temperature is regulated using a Lakeshore 331 controller to perform measurements between 200 – 300 K. The ideality factor (n) and saturation current density (J_0) is determined at each temperature (T) by rearranging the Shockley diode equation [12]. The gradient and intercept of an $\ln(J) - V$ plot is then used to find the ideality factor and saturation current density respectively by fitting to the exponential region, thus neglecting the effects of shunt and series resistance:

$$\ln(J) = \frac{q}{nkT}V + \ln(J_0) \tag{4.10}$$

The series resistance can be determined from the gradient of *JV* curves in forward bias prior to the onset of rollover effects. The back contact barrier height can then be determined from the method outlined by Bätzner et al [13], where the total series resistance arises from ohmic contributions ($R_{\Omega 0}$) which has a temperature dependence $\left(\frac{\partial R_{\Omega 0}}{\partial T}T\right)$ and from thermionic emission $\left(\frac{C}{T^2}e^{\frac{\phi_b}{kT}}\right)$ due to transport of carriers across a Schottky barrier of height ϕ_b, where C is a constant.

$$R_s = R_{\Omega 0} + \frac{\partial R_{\Omega 0}}{\partial T}T + \frac{C}{T^2}e^{\phi_b/kT} \tag{4.11}$$

The barrier height can then be estimated from the temperature dependence of the series resistance in instances where the depletion region of the back contact barrier does not overlap with that of the main junction.

4.4.3 External Quantum Efficiency

External quantum efficiency (EQE) measurements determine the ratio of photogenerated electrons that are collected by a solar cell to the number of incoming photons as a function of wavelength. This is achieved by measuring the spectral response (A W^{-1}) of a device and is converted to EQE by accounting for the charge of an electron and the energy of photons at a given wavelength:

$$EQE\ (\%) = \frac{electrons\ out}{photons\ in} = \frac{current/q}{power/hv} = SR \times \frac{hv}{q\lambda} \tag{4.12}$$

The J_{sc} of a solar cell can be determined from EQE measurements by integrating the quantum efficiency at each wavelength across suitable wavelengths, accounting for the spectral photon flux ϕ_λ at each wavelength in the AM1.5G spectrum, as shown in Figure 4.9b.

$$J_{sc} = -q \int_{\lambda_1}^{\lambda_2} EQE(\lambda)\, \phi_\lambda^{AM1.5G}\, d\lambda \tag{4.13}$$

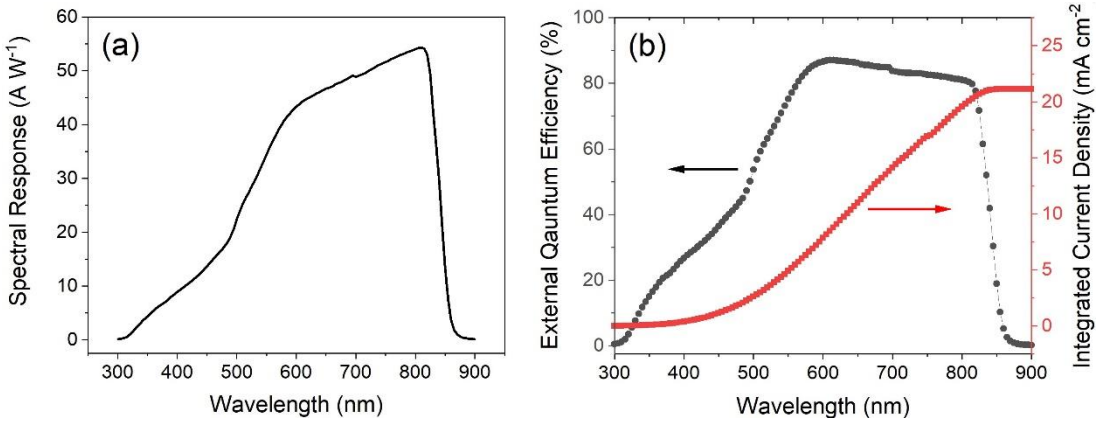

Figure 4.9: (a) Example of a spectral response curve which is measured directly as a function of wavelength and (b) external quantum efficiency, which is calculated from the spectral response and can be used to determine the expected short circuit current density as shown in equation (4.13)

Spectral response measurements were taken in this work using a Bentham PVE300 measurement system calibrated with a silicon photodiode and converted to EQE using BenWin$^+$ software. Data were taken at wavelengths between 300 – 900 nm using a monochromator to select photons from a dual xenon/quartz-halogen light source. The incoming light is chopped using a filter wheel and the photogenerated current measured using a lock-in amplifier. All measurements were performed without a white bias light and therefore the relatively low light intensity of the monochromatic light does not represent typical operating conditions for a solar cell, hence caution is necessary when interpreting data.

4.4.4 Capacitance Voltage

Capacitance voltage (*CV*) measurements were undertaken to determine the net doping density within the absorber layer of devices using a Solartron SI1260 impedance analyser to apply a 30 mV AC perturbation voltage over a DC bias voltage swept between -0.5 V to +0.5V. The *p-n* junction consists of a depletion region devoid of charge carriers, surrounded by a quasi-neutral region either side with N_A or N_D free carriers. This can therefore be modelled as a parallel plate capacitor with capacitance (C) related to the width of the depletion region (W):

$$C = \frac{\varepsilon A}{W} \tag{4.14}$$

Where A is the plate area and ε is the dielectric permittivity. The width of the depletion region of a *p-n* junction is dependent upon the applied bias voltage and is found by integrating Poisson's equation for both sides of the junction. Where the *p*-type and *n*-type regions have drastically different doping densities, such as in typical CdTe solar cells, the depletion region resides almost entirely in the material with lower doping density. In the case of an *p-n*$^+$ junction, the depletion width is given as:

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_A + N_D}{N_A\, N_D}\right) V_{bi} - V_{applied}} \approx \sqrt{\frac{2\varepsilon\,(V_{bi} - V_{applied})}{q\, N_A}} \tag{4.15}$$

Comparing equations (4.14) and (4.15) it can be seen that the capacitance across the *p-n* junction of a solar cell is related to the applied bias voltage ($V_{applied}$), and is described by the Mott-Schottky equation [14] :

$$\frac{1}{C^2} = \frac{2}{q\varepsilon A^2 N_A}(V_{bi} - V_{applied}) \tag{4.16}$$

By plotting $1/C^2$ vs $V_{applied}$, the acceptor density N_A is calculated from the gradient and the built-in voltage should correspond to the *x*-axis intercept.

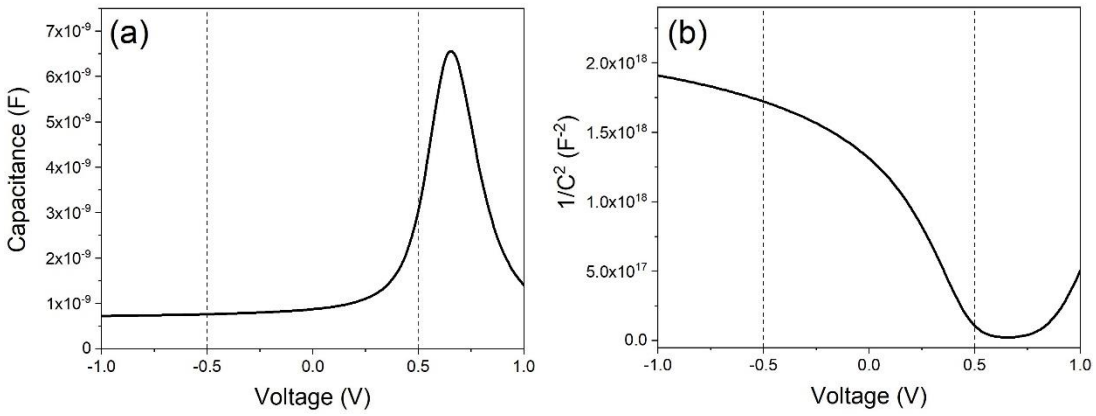

Figure 4.10: Example of (a) raw *CV* data typical for CdTe devices and (b) the corresponding Mott-Schottky plot. The region from -0.5 V to +0.5 V is highlighted to show the range used for subsequent analysis to avoid the effects of a non-ohmic back contact.

Figure 4.10 shows an example of the typical *CV* response for CdTe devices as well as the corresponding $1/C^2$ vs $V_{applied}$ plot. By comparing this to equation (4.16), it is seen that caution is required in interpreting Mott-Schottky analysis for CdTe solar cells, especially outside of a narrow voltage range close to zero bias. A non-ohmic back contact contributes a capacitance signal that results in a peak in *CV* plots at forward bias, as shown in Figure 4.10a, and therefore analysis is restricted to voltages between -0.5 V to +0.5 V to avoid this effect. However, even in this narrow voltage range devices deviate from the idealised behaviour predicted by equation (4.16). Instead of a linear $1/C^2$ response whereby the gradient can be used to calculate the net acceptor density and the intercept corresponds to the built-in voltage, Figure 4.10b shows a curve. This non-linearity means that it is not possible to accurately determine the built-in voltage from these measurements [15].

The non-linearity of the Mott-Schottky plot in Figure 4.10b also implies that N_A varies with applied voltage, leading to a characteristic 'U' shaped apparent carrier density profile as shown in Figure 4.11. Whilst the carrier density is indeed likely to vary to some extent throughout the device, a non-ohmic back contact, thin absorber layer and deep level defects can also contribute to the observed increase on both the left and right hand side of the curve minimum [16]. Therefore, in this work the acceptor concentration of devices is estimated from the minimum of the carrier density profile.

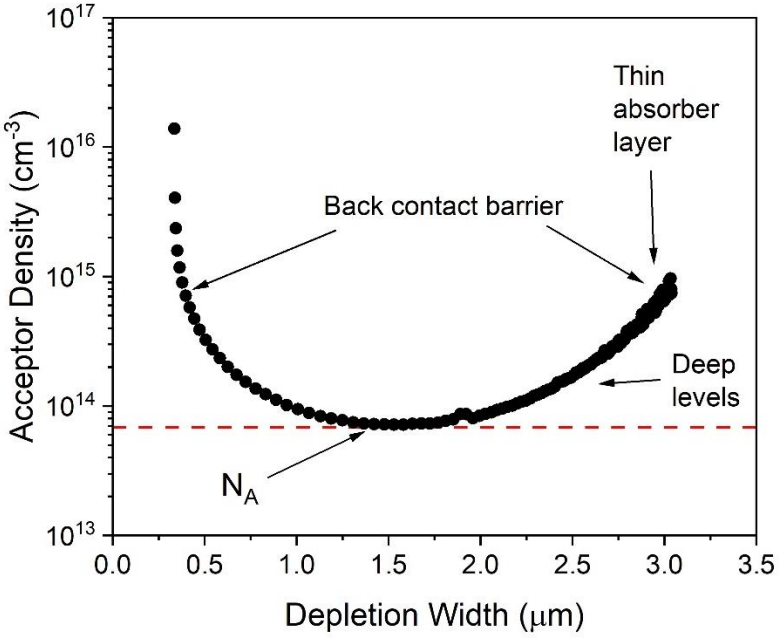

Figure 4.11: Example of CdTe carrier density profile indicating sources of non-ideal behaviour which contribute to artificially increased acceptor density, and the estimated net acceptor density for the bulk absorber layer in the device.

4.5 References

1. Amarasinghe, M. *et al.* Influence of CdTe deposition temperature and window thickness on CdTe grain size and lifetime after $CdCl_2$ recrystallization. *IEEE J. Photovoltaics* **8**, 600–603 (2018).

2. Mattox, D. M. Vacuum Evaporation and Vacuum Deposition. in *Handbook of Physical Vapor Deposition (PVD) Processing* 195–235 (Elsevier, 2010). doi:10.1016/b978-0-8155-2037-5.00006-x

3. Rockett, A. Thin Film Growth Processes. in *The Materials Science of Semiconductors* 455–503 (Springer US, 2008). doi:10.1007/978-0-387-68650-9_10

4. Mattox, D. M. Physical Sputtering and Sputter Deposition (Sputtering). in *Handbook of Physical Vapor Deposition (PVD) Processing* 237–286 (Elsevier, 2010). doi:10.1016/b978-0-8155-2037-5.00007-1

5. Barrett, C. S. & Massalski., T. B. Structure of metals : crystallographic methods, principles and data. (McGraw-Hill, 1966).

6. van der Heide, P. X-Ray Photoelectron Spectroscopy: An Introduction to Principles and Practices. X-Ray Photoelectron Spectroscopy: An Introduction to Principles and Practices (John Wiley and Sons, 2011). doi:10.1002/9781118162897

7. Rein, S. Theory of carrier lifetime in silicon. in Lifetime Spectroscopy: A Method of Defect Characterization in Silicon for Photovoltaic Applications **85**, 5–58 (Springer Verlag, 2005).

8. Major, J. D. *et al.* In-depth analysis of chloride treatments for thin-film CdTe solar cells. *Nat. Commun.* **7**, 13231 (2016).

9. Metzger, W. K., Ahrenkiel, R. K., Dashdorj, J. & Friedman, D. J. Analysis of charge separation dynamics in a semiconductor junction. *Phys. Rev. B - Condens. Matter Mater. Phys.* **71**, 035301 (2005).

10. Zanatta, A. R. Revisiting the optical bandgap of semiconductors and the proposal of a unified methodology to its determination. *Sci. Rep.* **9**, 11225 (2019).

11. Tauc, J., Grigorovici, R. & Vancu, A. Optical Properties and Electronic Structure of Amorphous Germanium. *Phys. status solidi* **15**, 627–637 (1966).

12. Shockley, W. The theory of p-n junctions in semiconductors and p-n junction transistors. *Bell Syst. Tech. J.* **28**, 435–489 (1949).

13. Bätzner, D. L., Öszan, M. E., Bonnet, D. & Bücher, K. Device analysis methods for physical cell parameters of CdTe/CdS solar cells. *Thin Solid Films* **361**, 288–292 (2000).

14. Sze, S. M. & Ng, K. K. *Physics of semiconductor devices*. (Wiley-Interscience, 2007).

15. Mingebach, M., Deibel, C. & Dyakonov, V. Built-in potential and validity of the Mott-Schottky analysis in organic bulk heterojunction solar cells. *Phys. Rev. B - Condens. Matter Mater. Phys.* **84**, 153201 (2011).

16. Li, J. V. *et al.* Theoretical analysis of effects of deep level, back contact, and absorber thickness on capacitance–voltage profiling of CdTe thin-film solar cells. *Sol. Energy Mater. Sol. Cells* **100**, 126–131 (2012).

Chapter 5

A comparison of CdTe solar cells having different organic back contacts

Part of this chapter is based on work that has previously been published as:

T. P. Shalvey, L.J. Phillips, K. Durose and J. D. Major, "A comparison of organic back contact materials for CdTe solar cells", in the 45th IEEE Specialists' Photovoltaics Conference Hawaii (2018), 10.1109/PVSC.2018.8547725

5.1 Introduction

The issue of forming an ohmic contact to *p*-CdTe due to its high electron affinity is well known and must be mitigated to increase the open circuit voltage and fill factor of CdTe PV devices towards their Shockley-Queisser limit [1]. Considerable research efforts have focussed on minimising the effect of any resultant Schottky barrier at the back contact which acts in opposition of the main junction (section 2.33). Strategies to overcome this are detailed in section 3.8 and typically include etching the back surface, narrowing the barrier with extrinsic dopants such as copper to produce a p^+ region, or depositing an intermediate layer between the CdTe and metal to improve band alignment and therefore aid hole extraction [2–4]. These interlayers deposited at the back contact have almost exclusively focussed on inorganic semiconductors such as ZnTe, Te, Sb_2Te_3 and MoO_x [5–8]. In contrast, reports of organic contacts to CdTe are much less common despite offering a potentially promising avenue of exploration, with investigations limited to P3HT, PEDOT:PSS, PCBM, polyaniline and spiro-OMeTAD [9–14].

Consideration of organic semiconductors opens an enormous range of possible back contact materials which have received very little attention to date. They offer the possibility of precisely tailoring the optoelectronic properties of contact layers to serve multiple purposes simultaneously, such as aiding hole extraction with a suitable valence band alignment whilst repelling electrons away from the back contact with a large conduction band offset to reduce

recombination. Organic compounds such as P3HT [9] and polyaniline [14] have also shown promise as pinhole blocking layers which can improve device uniformity and allow thinner CdTe layers to be deposited, which is favourable from both a device performance and material usage perspective [15]. Tuning of the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) positions of organic semiconductors is possible with the addition of functional groups to the side chain of polymers, and molecular doping affords control over the conductivity of layers [16] allowing precise optimisation in such a way that is more challenging within the limited parameter space afforded by inorganic contacts. Meanwhile the physical dimensions of even the smallest organic molecules suggests that diffusion into the CdTe layer will be avoided, in contrast to common inorganic contact layers which often include copper which migrates towards the front contact during operation [3].

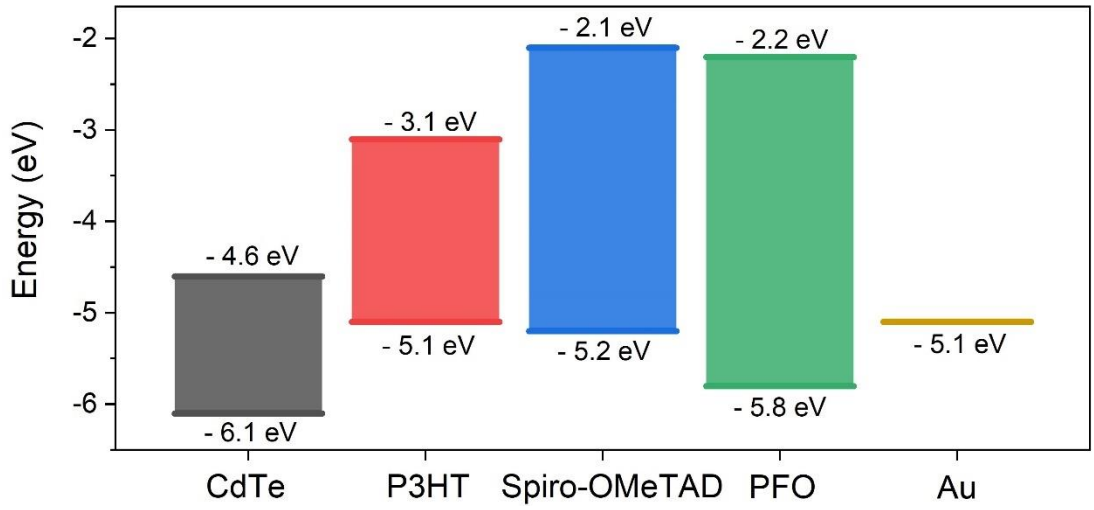

Figure 5.1: Diagram showing the CBM and VBM of CdTe compared to HOMO and LUMO positions of P3HT, spiro-OMeTAD and PFO as well as the work function of Au. The band positions for each material are taken from literature values [9,17]

Three different organic semiconductors are assessed here as potential hole transport layers for the back contact of CdTe solar cells, namely poly(3-hexylthiophene-2,5-diyl) (P3HT), (N^2,N^2,N^2,N^2,N^7,N^7,N^7,N^7-octakis(4-methoxyphenyl)-9,9–spirobi[9H-fluorene]-2,2,7,7-tetramin (spiro-OMeTAD) and poly(9,9-di-n-octylfluorenyl-2,7-diyl) (PFO). These compounds were identified based on having HOMO positions between the valence band maximum (VBM) of CdTe and work function of Au, as shown in Figure 5.1. It is anticipated that such staggered alignments may aid hole extraction. After a brief optimisation of each device structure, these are then compared to a simple Au-only back contact to determine their effectiveness at reducing the back contact barrier and also to evaluate any pinhole blocking effects to improve the average performance of devices.

5.2 Optimisation of contact layers

5.2.1 Introduction

To allow a meaningful comparison of the effect of each organic layer on device performance, a brief optimisation of each back-contact structure was performed to determine the best processing conditions in each case. All the organic layers were deposited via spin coating, with variables such as solution volume, spin speed, dopant concentration and post deposition annealing studied to identify suitable processing conditions for each device structure. The bulk of these results are omitted for brevity, however an overview of the optimisation studies of critical processing steps which were found to have a substantial impact on device performance are presented here to demonstrate the effect of changing key variables during the processing of the devices with different contact structures.

5.2.2 Device fabrication

CdTe solar cells were fabricated in superstrate configuration onto TEC15M glass substrates, which include a SnO_2:F TCO layer as well as an intrinsic SnO_2 HRT layer. After substrate cleaning, CdS was deposited via sputtering in 5 mTorr Ar at a substrate temperature of 200°C and power density of 1.32 W cm^{-2} for 30 min, which results in a film thickness of 100 nm. CdTe was deposited via CSS at source and substrate temperatures of 610°C and 510°C respectively under 30 Torr nitrogen resulting in a film thickness which varied between 4 – 5 μm across a 5×5 cm^2 plate. Samples then underwent a 15 second NP etch before and after a 20 min $MgCl_2$ treatment carried out at 410°C.

Solutions of each organic material were prepared under a N_2 atmosphere by dissolving an appropriate amount of material into 1 ml of chlorobenzene. These solutions were then heated to 50°C for 1 hour and stirred until fully dissolved, and once cool were dynamically spin coated onto the etched surface of the CdTe devices. The exact processing parameters are varied as part of the optimisation process of each organic contact and therefore further details of the solution preparation, spin coating parameters are given in the relevant section. Where samples required a further annealing step, this was performed in an air ambient.

Following preparation of the organic layer, a 50 nm Au layer was deposited onto the back surface of devices through a mask to define nine 0.25 cm^2 cells per device. Electrical contact to the underlying TCO layer was made by mechanical scribing of the CdTe and swabbing HCl to remove the CdS layer.

5.2.3 P3HT – Anneal duration

The use of P3HT as an interface layer for CdTe solar cells has previously been reported [9], showing a beneficial effect on peak performance for Cu-free devices as a result of a lower barrier height at the back contact. It also showed an improved average efficiency irrespective of Cu inclusion by compensating for the deleterious effects of pinholes by preventing shunting. A similar approach is used here to compare to this prior work, whilst further exploring the parameter space to determine the key processing variables to ensure high efficiency. Several device series covering a range of P3HT deposition conditions were fabricated in this work to determine the optimal processing parameters for variables such as solution concentration, volume, and annealing conditions. This establishes a baseline demonstrating an effective organic contact which can then be compared against other potential organic contacts. The effect of annealing devices with a P3HT layer spin coated from a 10 mg/ml solution at 4000 rpm is shown here, since this made the most difference to device performance and was found to be essential to obtain high efficiencies.

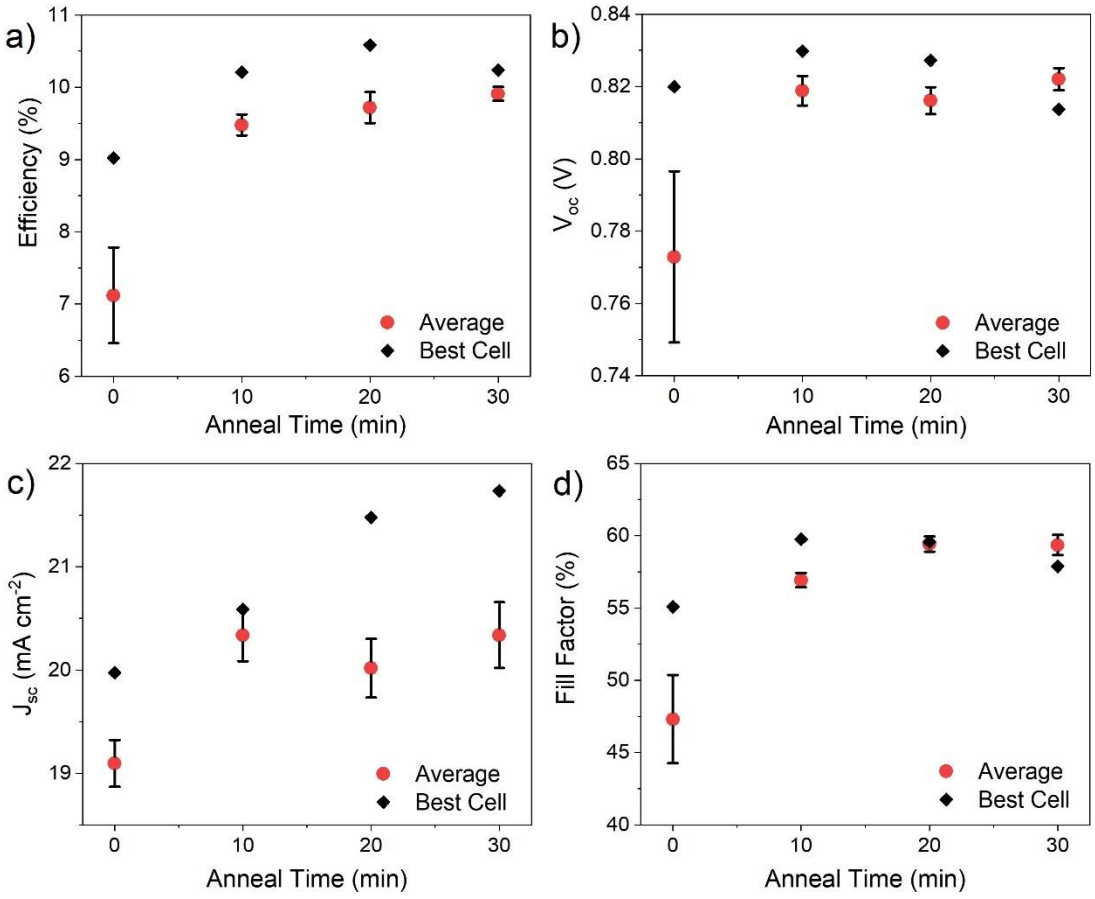

Figure 5.2: Performance parameters of CdTe devices with P3HT deposited at the back surface and annealed at 150°C for between 0 – 30 min in air prior to contacting with 50 nm Au. The average efficiency (a), open circuit voltage (b), short circuit current density (c) and fill factor (d) is given with error bars showing the standard deviation from nine cells per device, as well as the parameters corresponding to the highest efficiency cell in each case.

The performance parameters of devices as a function of annealing time at 150°C are given in Figure 5.2. Without post-deposition annealing, devices show poor performance compared to the annealed P3HT layers primarily due to lower fill factor and short circuit current. A brief anneal in air at 150°C increases both average and peak performance, with smaller error bars implying more uniform device performance. Whilst the peak V_{oc} remains relatively constant between the devices, average V_{oc} is improved by around 50 mV suggesting improved uniformity. There is also a reduction in series resistance with longer anneal times which leads to an increase in fill factor and J_{sc}. The lower series resistance likely arises from improved orientation of the P3HT layer, which is highly disordered upon deposition and therefore displays low mobility. Upon annealing of P3HT films the π–π stacking distance is decreased [18,19], implying increased crystallinity which would in turn be expected to increase mobility and hence conductivity. Furthermore, the band gap of regioregular P3HT has been shown to have a weak dependence on annealing for samples [18]. The effectiveness of an interface layer is likely dependent upon the band alignment at the back contact since this will determine the efficiency of hole extraction (Figure 5.1), and therefore any change in HOMO position of the P3HT with annealing might also play some role in the improved device performance.

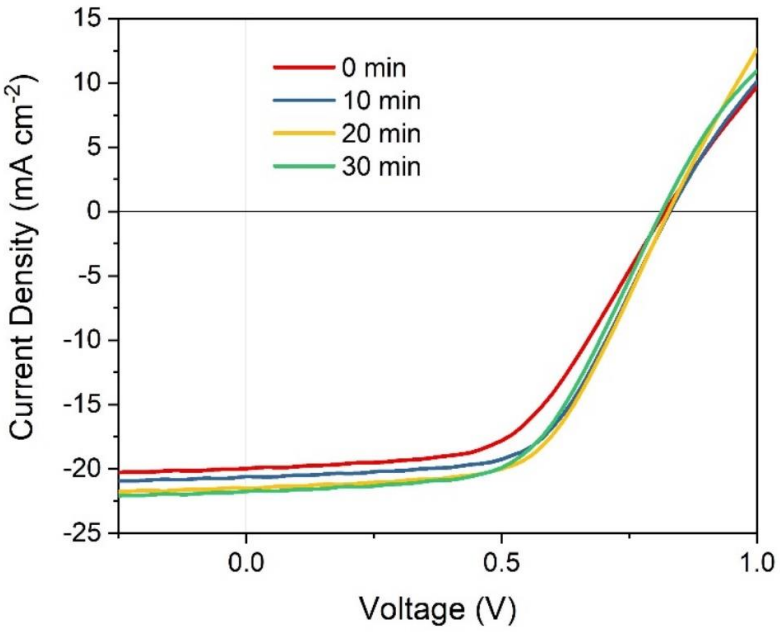

Figure 5.3: *JV* curves from the highest efficiency contact of CdS/CdTe devices with P3HT contacts, annealing in air for up to 30 mins.

Figure 5.3 shows the *JV* curves corresponding to the highest efficiency contact from the devices shown in Figure 5.2. All devices have a similar V_{oc}, whilst the J_{sc} increases with annealing temperature. There is a substantial improvement in fill factor apparent for devices that were annealed following deposition of the P3HT layer due to lower series resistance, irrespective of anneal time. All curves show a slight rollover effect at forward bias above V_{oc}. This is most noticeable for the device annealed for 30 min, however it is not clear whether this

represents a difference in the barrier height compared to the other devices. This device has a slightly lower V_{oc} due to an excessive anneal time, which could imply a lower built in voltage that is more sensitive to the barrier at the back contact.

5.2.4 Spiro-OMeTAD – Doping and annealing

Spiro-OMeTAD is a commonly used as a hole contact in perovskite based solar cells and has also shown promise in CdTe based devices. It has previously been incorporated into nanocrystalline CdTe solar cells as a hole transport material to replace MoO_x [13]. This enabled an increase in V_{oc} and J_{sc}, which is attributed to a reduction in back contact recombination due to surface dipole effects, however no further investigations of such contacts have been reported. In this work, spiro-OMeTAD is incorporated into a more typical CdTe device structure. It has a similar HOMO position as P3HT, therefore might be expected to produce a staggered band alignment at the back contact and prove similarly effective as a contact.

Initial optimisation runs undertaken in this work involved simply dissolving spiro-OMeTAD in chlorobenzene and spin coating from various concentrations over a range deposition parameter. These early attempts proved unsuccessful due to high resistivity of the spiro-OMeTAD irrespective of processing conditions. However, its widespread use as a hole transport material in perovskite solar cells means that there is a wealth of literature on processing routes to improve the performance of the layer. The addition of lithium bis(trifluoromethanesulfonyl)imide (Li-TFSI) and 4-*tert* butyl pyridine (tBP) to spiro-OMeTAD is a typical method of improving conductivity via *p*-type doping for use in perovskite and dye-sensitised solar cells [20,21], and therefore a similar approach has been adopted here.

Figure 5.4 shows the performance parameters taken from *JV* measurements of devices with a spiro-OMeTAD layer deposited between the CdTe back surface and Au contacts. The concentration of the spiro-OMeTAD and tBP was kept constant in each case at 10 mg/ml and 13 μl/ml in chlorobenzene respectively. Li-TFSI was dissolved in acetonitrile at a concentration of 500 mg/ml. An appropriate amount (0 – 10 μl/ml) was then mixed with the spiro-OMeTAD and tBP solution to achieve a Li-TFSI concentration of 0 – 5 mg/ml. These were then stirred for 60 min at 50°C to ensure the components were well mixed, before spin coating onto the CdTe back surface. Preliminary experiments highlighted the importance of post deposition annealing (see Figure 5.6) of the doped spiro-OMeTAD layer. Therefore devices were also annealed at 150°C for 20 minutes prior to Au deposition, with annealing conditions optimised for highest efficiency.

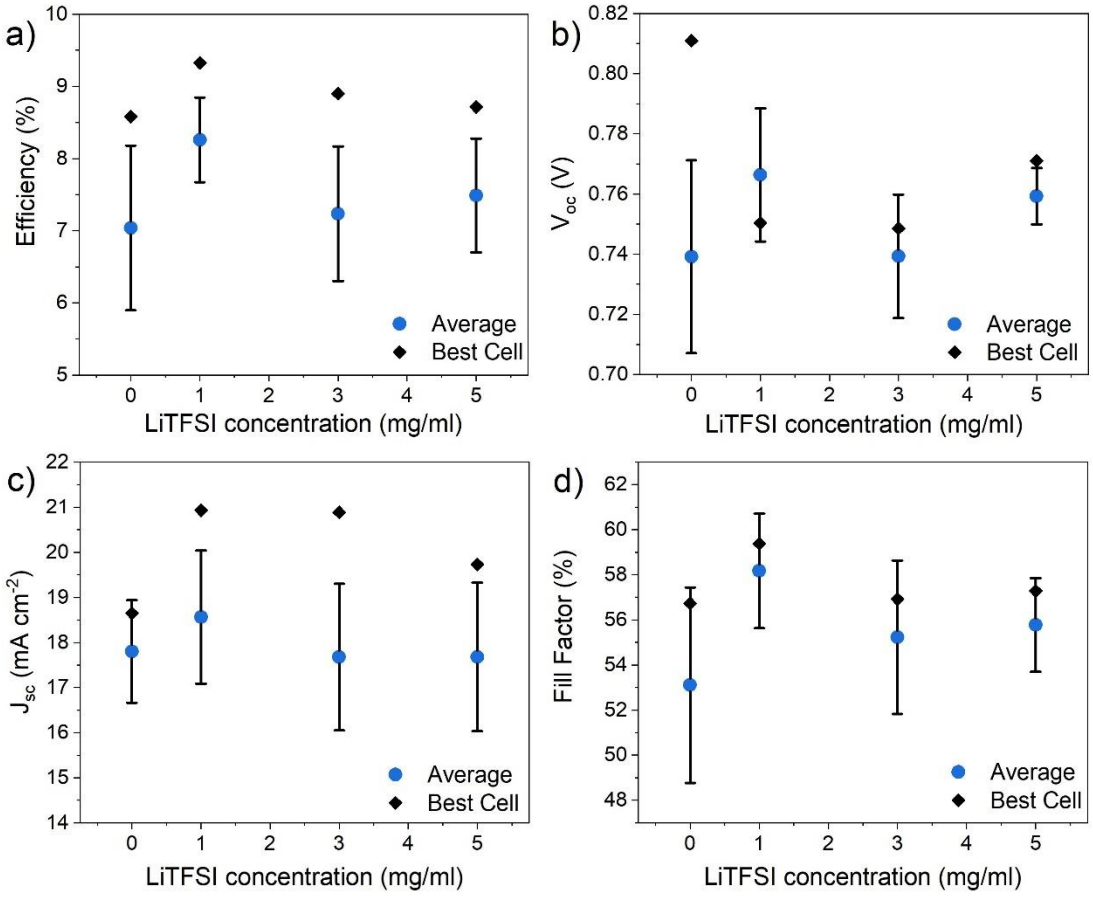

Figure 5.4: Performance parameters of devices with a back contact spin coated from a solution of 10 mg/ml spiro-OMeTAD, 13 µl/ml tBP and Li-TFSI concentration varied between 0 – 5 mg/ml in chlorobenzene. The average efficiency (a), open circuit voltage (b), short circuit current density (c) and fill factor (d) is given with error bars showing the standard deviation from nine cells per device, as well as the parameters corresponding to the highest efficiency cell in each case.

A small increase in average and peak efficiency is observed in Figure 5.4 upon inclusion of Li-TFSI compared to devices with undoped spiro-OMeTAD. This is most noticeable for 1 mg/ml due to higher short circuit current density and fill factor. This is a result of a significant reduction in series resistance from 17.4 Ω cm^{-2} to 8.4 Ω cm^{-2} for the highest efficiency cell on the 0 mg/ml and 1 mg/ml devices respectively. However, this is accompanied by a reduction in the peak open circuit voltage, which is decreased for all devices with a doped spiro-OMeTAD layer. As a result, there is a more modest increase in device efficiency than might be expected. This could potentially be due to excessive lithium migration towards the front contact when high Li-TFSI concentrations are used in device processing.

Figure 5.5 shows the measured *JV* curves corresponding to the highest efficiency contact from the devices shown in Figure 5.4. The 0 mg/ml device displays strong rollover at forward bias which is more severe than typically observed for devices without an interface layer. This may be due to the poor conductivity of undoped spiro-OMeTAD meaning carriers are required to tunnel through the resistive organic layer as well as the existing Schottky barrier. This rollover

is not apparent in the devices with a doped contact layer, suggesting improved carrier transport and potentially a lower barrier height when Li-TFSI is included in the device structure. The fill factor is improved due to lower series resistance and is accompanied by an increase in J_{sc}. Although doping the spiro-OMeTAD increases the overall efficiency of the cells, this is accompanied by a reduction in V_{oc}. Spin coating from solutions with ≥3 mg/ml Li-TFSI causes visibly poor film coverage which is likely to be due to its hygroscopic nature and may contribute to the reduced performance. Further optimisation of the concentration of tBP, which helps control the morphology of spiro-OMeTAD layers for perovskite solar cells [21], may overcome this.

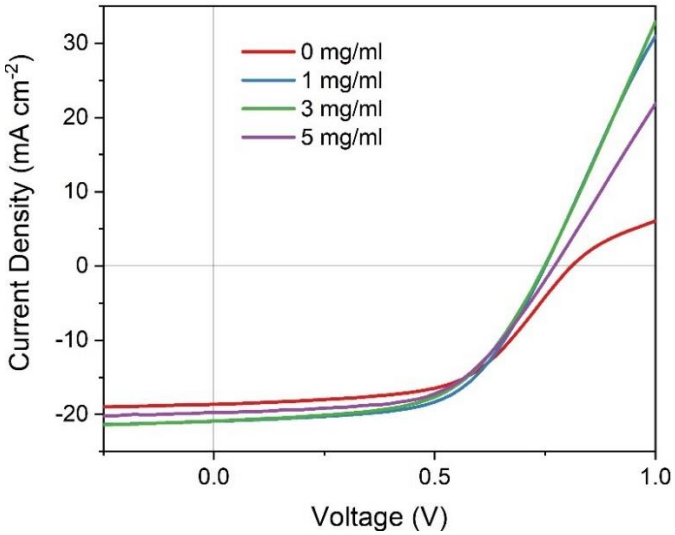

Figure 5.5: *JV* measurements of the highest efficiency contact from CdTe devices with a spiro-OMeTAD back contact doped with 0 – 5 mg/ml Li-TFSI.

It is noted that the fabrication procedure for the spiro-OMeTAD contacts described above is the product of an extensive optimisation procedure. Preliminary attempts to incorporate doped spiro-OMeTAD layers into CdTe devices followed a similar method to that used in perovskite solar cells [22–24]. This involved a complex post deposition process to encourage *p*-type doping of the layer by spin coating in air, drying films at room temperature in a nitrogen atmosphere before being moved to a desiccator for 24 hr in the dark. However, initial efforts to measure the efficiency of these devices were hindered by inconsistent results whereby device performance changed considerably over the course of a measurement. Figure 5.6a exemplifies this, demonstrating how the efficiency of a CdTe device with a doped spiro-OMeTAD layer processed in a way typical for perovskite solar cells changes significantly over a 30 minute period when placed under continuous 1 sun illumination. A typical cell with a simple Au contact is compared to cells with 100 µl of 10 mg/ml spiro-OMeTAD solution doped with 1 mg/ml Li-TFSI spin coated onto back surface at 3000 and 4000 rpm, whereby higher spin speeds result in a thinner layer. A device with a doped spiro-OMeTAD layer followed by a post deposition annealing step at 150°C for 20 min in air is also shown for comparison.

The efficiency of cells containing spiro-OMeTAD without annealing increases rapidly for ~5 mins before levelling off, with the effect much more noticeable for slower spin speeds. This was only observed when Li-TFSI was added to the spiro-OMeTAD solution and therefore appears to be linked to the doping mechanism. This mechanism is reported to be light dependent and involve a two-step process whereby the spiro-OMeTAD initially undergoes a reversible oxidation reaction followed by subsequent doping with Li-TFSI [20]. It is therefore reasonable to consider the role of the illumination from the solar simulator and whether this stabilisation period can be eliminated. Whilst the continuous illumination itself may have some effect on the doping process, since the stage is not temperature controlled it will also result in some degree of low temperature annealing from the intense radiation. Following the introduction of a 20 min, 150°C post deposition air annealing step during the device fabrication, the initial increase is almost entirely eliminated and cells maintain much higher efficiency as shown in Figure 5.6a.

Figure 5.6b gives more detail of the effect of the annealing step, showing the influence of anneal duration on device efficiency and series resistance. Here, devices do not undergo the convoluted post deposition doping process used in perovskite literature but are instead subject to an anneal at 150°C in air immediately following the deposition of the spiro-OMeTAD layer. Annealing devices causes a sharp increase in efficiency which is strongly correlated with a lowering of series resistance leading to improved fill factor. Not only does this annealing step remove instabilities observed during subsequent measurements and the need for stabilisation, but annealed devices also reach higher efficiency than those left to stabilise under illumination and those without Li-TFSI.

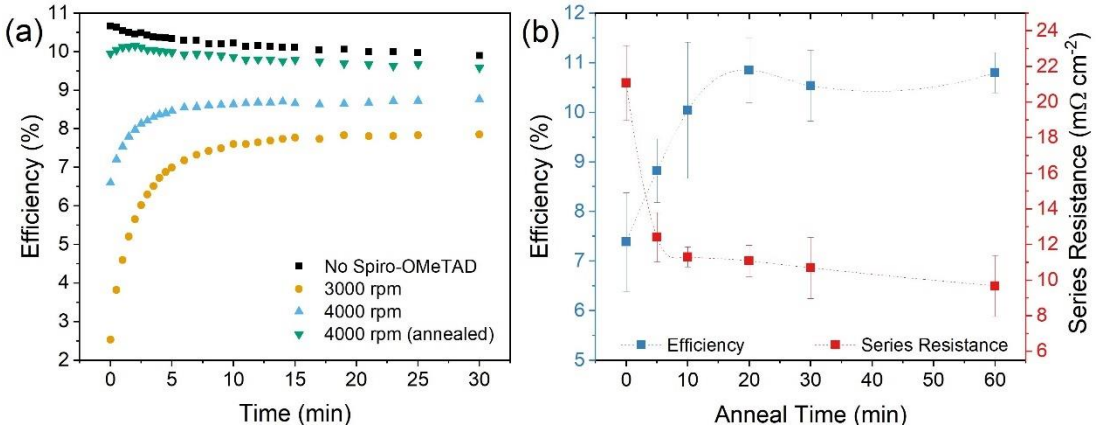

Figure 5.6: (a) Efficiency of CdTe devices repeatedly measured over a 30 min duration when continuously exposed to AM1.5G illumination. Devices with a Li-TFSI doped spiro-OMeTAD layer deposited at different spin speeds and anneal conditions are compared to a device with a standard Au contact. (b) shows the effect of anneal duration on the average efficiency and series resistance of CdTe devices with a Li-TFSI doped spiro-OMeTAD layer spin coated at 4000rpm and annealed at 150°C in air

5.2.5 PFO – Solution concentration

PFO is a common organic polymer that is widely used in organic PV and OLED devices [25,26]. It has a HOMO position of -5.8 eV [17], which is well matched to the VBM of CdTe and therefore may be expected to facilitate hole extraction in a similar manner to the ZnTe based contacts [5]. A range of solution concentrations, spin coating parameters and post deposition annealing treatments were studied to determine the optimal processing parameters for PFO contacts, however in each case this led to a decrease in device efficiency compared to a simple Au contact. In general, the efficiency reduction was proportional to the thickness of the PFO layer. The effect of solution concentration on CdTe devices is shown in Figure 5.7, and is representative of typical observations for PFO contacts made throughout the optimisation of this device structure. This shows the performance parameters taken from *JV* measurements of CdTe devices with 100 µl of chlorobenzene solutions containing 5 – 15 mg/ml PFO spin coated at 4000 rpm onto the back surface compared to an Au-only device without any spin coated layer (i.e. 0 mg/ml). No further anneals were performed before Au contacting.

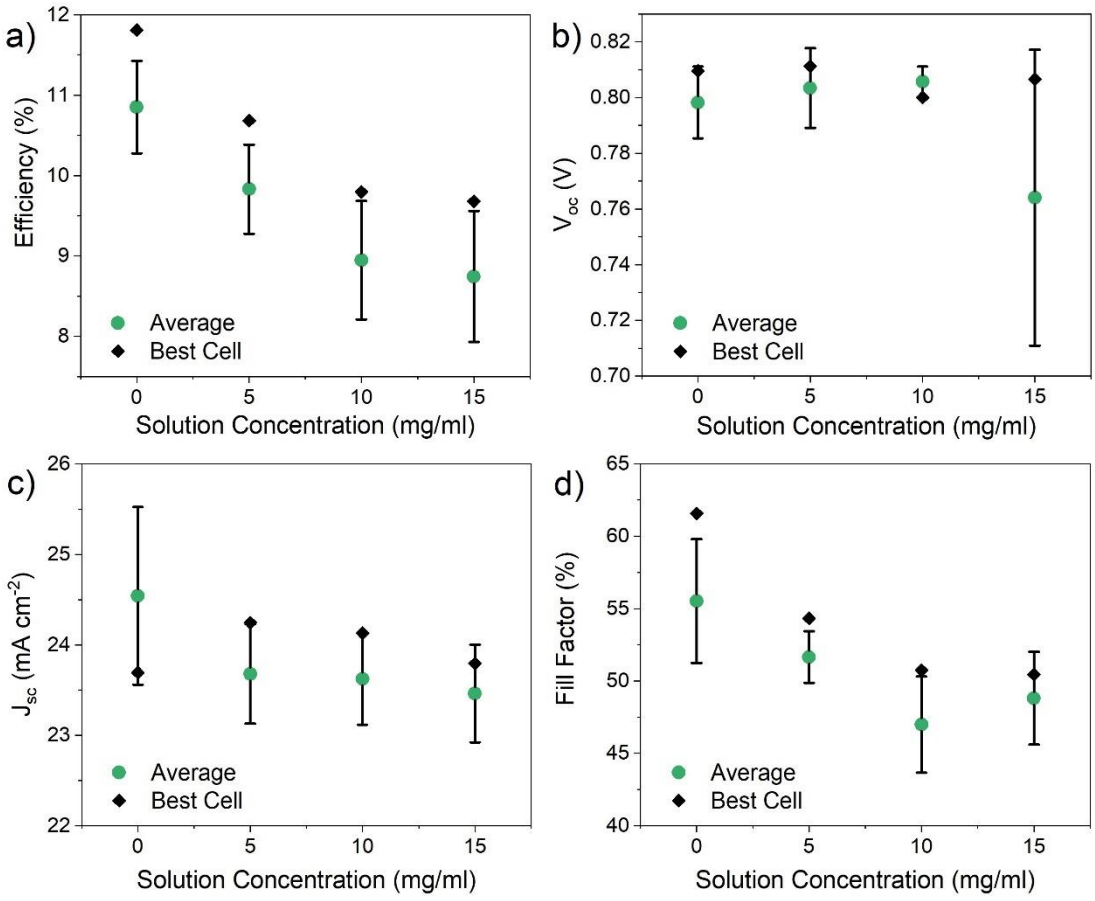

Figure 5.7: Performance parameters of CdTe devices with 100 µl PFO spin coated onto the back surface from solution concentrations between 0 – 15 mg/ml in chlorobenzene at prior to contacting with 50 nm Au. The average efficiency (a), open circuit voltage (b), short circuit current density (c) and fill factor (d) is given with error bars showing the standard deviation from nine cells per device, as well as the parameters corresponding to the highest efficiency cell in each case.

It can be seen from Figure 5.7 that in all instances where PFO was applied at the back contact, device efficiency is progressively lowered. Both average and peak efficiency decrease with increasing film thickness. This reduction in efficiency is largely attributable to an increase in series resistance which limits fill factor, with increased series resistance and therefore lower fill factor responsible for most of the loss. Whilst the average J_{sc} is reduced for devices with a PFO layer, there is little difference for the highest efficiency devices. The V_{oc} is insensitive to the PFO solution concentration, although the average V_{oc} for the 15 mg/ml device is lowered considerably by a single poorly performing cell. Similar results were found for lower spin speeds and increased solution volume, which will result in thicker PFO films, whilst post deposition annealing has little effect overall. Indeed, performance was reduced for all device series with a PFO contact regardless of processing conditions.

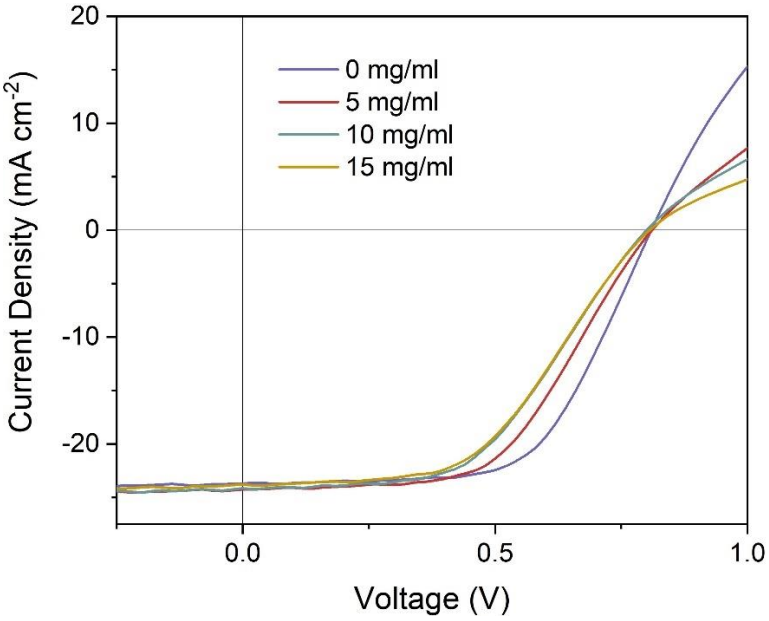

Figure 5.8: *JV* curves for the highest efficiency contact from CdTe devices with 0 – 15 mg/ml solutions of PFO in chlorobenzene spin coated onto the back surface prior to metallisation with Au contacts

Figure 5.8 shows the *JV* curves corresponding to the highest efficiency contacts from devices in described in Figure 5.7. The addition of PFO to the back contact causes a significant increase in series resistance thereby reducing fill factor. The current limiting effect above V_{oc} is worsened for devices with a PFO contact, with the extent of rollover correlated with the solution concentration. However, it is unclear whether this enhanced rollover is a symptom or the cause of the increased series resistance. Although PFO would seem an ideal candidate based on its predicted band alignment to CdTe, these results show no benefit to device performance, instead acting only to increase resistivity and thereby lower efficiency. Further optimisation incorporating dopants such as F_4-TCNQ offer a potential route to increasing the conductivity of PFO [27] and thereby improving its performance as a contact layer to CdTe in a similar manner to that shown for spiro-OMeTAD layers in section 5.2.4.

5.3 Comparison of organic contacts

5.3.1 Introduction

Having determined suitable processing conditions for each of the organic back contact layers, a device series was fabricated to directly compare the effect of each contact structure on performance. The impact on individual cell performance and the electrical barrier height is examined for each contact structure, which primarily motivates the use of an interfacial back contact layer. The effect of these organic layers on the average device efficiency is also investigated in detail, since previous reports have shown some organic layers such as P3HT [9] and polyaniline [14] to be effective in blocking pinholes and other non-uniformities that would otherwise be detrimental to average performance. These factors were investigated by using deliberately inhomogeneous CdTe films and comparing the dependency of device performance on absorber layer thickness. In this way, these organic contacts can be assessed as both contact layers to simultaneously aid hole extraction and block pinholes. Although PFO did not appear to show any benefit in device performance during optimisation studies, it remains worthy of investigation here due to the potential for pinhole blocking effects.

5.3.2 Device fabrication

Devices were grown on TEC15 substrates, onto which 100 nm CdS was sputtered under 5 mTorr Ar at a power density of 1.32 W/cm^{-2} and substrate temperature of 200°C. CdTe was then deposited via CSS under 30 Torr nitrogen at source and substrate temperatures of 610°C and 510°C respectively. Whilst some variation in CdTe thickness is routinely observed during standard CSS depositions, this non-uniformity was intentionally exaggerated by placing the source material to sit underneath one side of the 5×5 cm^2 plate. This resulted in a thickness gradient between 1.5 – 4.5 μm and therefore allows a range of CdTe thicknesses to be examined from a single deposition. This enables the ability of the organic layers to block pinholes to be examined in tandem to device performance, since pinhole blocking will be more pronounced for thinner samples. Four identical 5×5 cm^2 plates were fabricated and each subjected to a $MgCl_2$ treatment at 410°C with a 15 second pre- and post-treatment NP etch. Layers of P3HT, spiro-OMeTAD and PFO were deposited onto three of these samples, with the remaining sample left uncoated. All organic layers were deposited from 100 μl of the relevant 10 mg/ml solution in chlorobenzene at 4000 rpm. The spiro-OMeTAD solution also contained 1 mg/ml Li-TFSI (added via a 500 mg/ml solution in acetonitrile) and 13 μl/ml tBP. Both the P3HT and spiro-OMeTAD samples underwent a 20 minute anneal in air following deposition, whereas the PFO sample did not. A 50 nm Au layer was then evaporated through

a 0.25 cm^2 shadow mask to define 36 cells per device. Each cell was also mechanically scribed around each contact to prevent current collection from outside of the defined device area.

5.3.3 Comparison of device performance

Figure 5.9 compares the performance parameters of 36 cells from each of the devices having either organic or a simple Au contact (control). There is significant variation in performance, which is typical for all devices grown during this work due to inhomogeneities in the CSS-grown CdTe, however is particularly noticeable within this dataset due to the intentional thickness gradient of the absorber layer. A full assessment of the ability of these organic layers to block pinholes is given in section 5.3.4, however from Figure 5.9 it is clear that the Au only contact shows two distinct groups of datapoints whereby some cells give reasonable efficiency whilst others show virtually no photovoltaic performance. The latter may be presumed to have shunted due to pinholes in the CdTe.

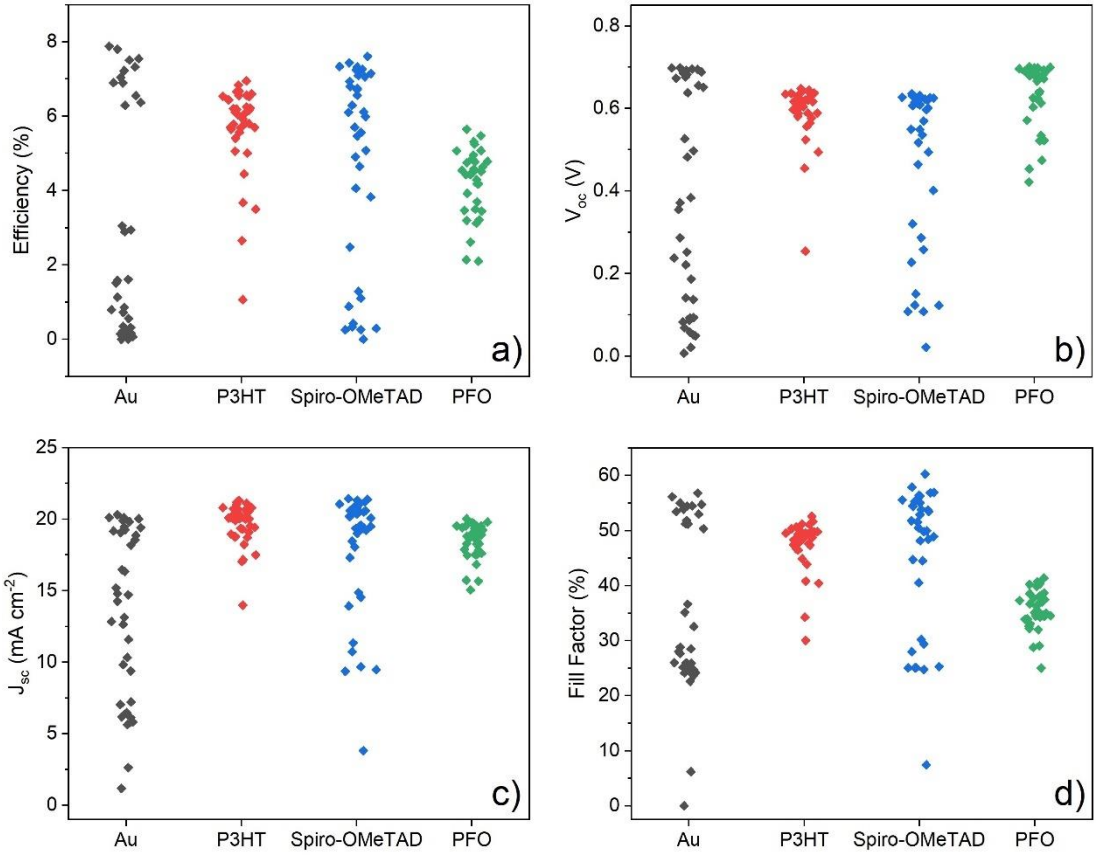

Figure 5.9: Performance parameters of solar cells with Au, P3HT, spiro-OMeTAD or PFO back contacts. The individual datapoints from 36 cells per device for (a) efficiency, (b) open circuit voltage, (c) short circuit current density and (d) fill factor are shown

As seen in Figure 5.9, the addition of any of the organic contact layers reduces the peak efficiency of devices compared to Au. This is a minor effect for spiro-OMeTAD but pronounced in the case of PFO. However, the average efficiency, and indeed nearly all average performance parameters, increases with the addition of any of the organic layers as shown in Table 5.1, which compares the average and peak performance of each of the device structures. The P3HT contact results in a much tighter distribution of all datapoints compared to the control device, with a reduced V_{oc} and fill factor partially offset by higher J_{sc} lowering peak performance from 7.88% to 6.94%. The spiro-OMeTAD device also produces a similar distribution of 'working' and 'shunted' cells as with the Au-only device. However, fewer of the spiro-OMeTAD cells are completely shunted and therefore have a higher average efficiency. As with P3HT, lower V_{oc} is partially offset by higher J_{sc}, however the fill factor of spiro-OMeTAD devices is also increased compared to Au-only devices due to a lower series resistance leading to similar peak efficiency. The device containing a PFO layer shows a tight distribution of all performance parameters, however efficiency is considerably lower than for the other device structures as a result of lower fill factor.

Table 5.1: Average and peak performance parameters of CdTe solar cells with Au, P3HT, spiro-OMeTAD or PFO contacts, taken from 36 cells per device, corresponding to the individual datapoints shown in Figure 5.9

Contact	Efficiency (%)	V_{oc} (V)	J_{sc} (mA cm^{-2})	Fill Factor (%)
Au				
Average:	3.11 ± 3.17	0.376 ± 0.265	13.67 ± 5.84	35.21 ± 15.35
Peak:	7.88	0.698	20.11	56.15
P3HT				
Average:	5.67 ± 1.23	0.593 ± 0.072	19.63 ± 1.46	47.62 ± 4.65
Peak:	6.94	0.643	21.12	51.09
Spiro-OMeTAD				
Average:	4.73 ± 2.70	0.471 ± 0.200	17.78 ± 4.46	45.43 ± 13.26
Peak:	7.61	0.626	21.38	56.88
PFO				
Average:	3.99 ± 1.31	0.600 ± 0.159	17.64 ± 3.64	34.49 ± 7.17
Peak:	5.65	0.701	20.03	40.25

JV curves from the highest performing contacts for devices with Au, P3HT, spiro-OMeTAD and PFO contacts are shown in Figure 5.10. The principal motivation for including these

interface layers at the back contact of CdTe solar cells is to reduce the Schottky barrier height which manifests as rollover in forward bias. Figure 5.10 shows that whilst the device containing P3HT shows very little rollover, it persists and is possibly worsened in the spiro-OMeTAD and PFO containing devices compared to the control device with an Au contact. However, whilst observation of rollover can be useful in diagnosing the presence of a contact barrier, it is a crude indicator of barrier height and therefore detailed discussion of this is deferred until presentation of temperature dependent *JV* measurements later in this section.

It should be noted that despite the reduced V_{oc} of devices with P3HT and spiro-OMeTAD contacts in Figure 5.10, this does not appear to be a fundamental limit on the efficiency since other authors show similar or improved V_{oc} with similar device structures [9,13], and indeed such observations have been made elsewhere in this work (e.g. Figure 5.2 and Figure 5.4). It would therefore appear that this V_{oc} loss may be caused by some unknown parameter during processing, for example a delay between etching the CdTe and depositing the organic layer could cause oxidation of the back surface. Therefore, it is likely that further refinement of the processing conditions would lead to improved performance. Nonetheless, the results in Figure 5.10 correspond to a single device series and so are included to provide a complete, consistent dataset.

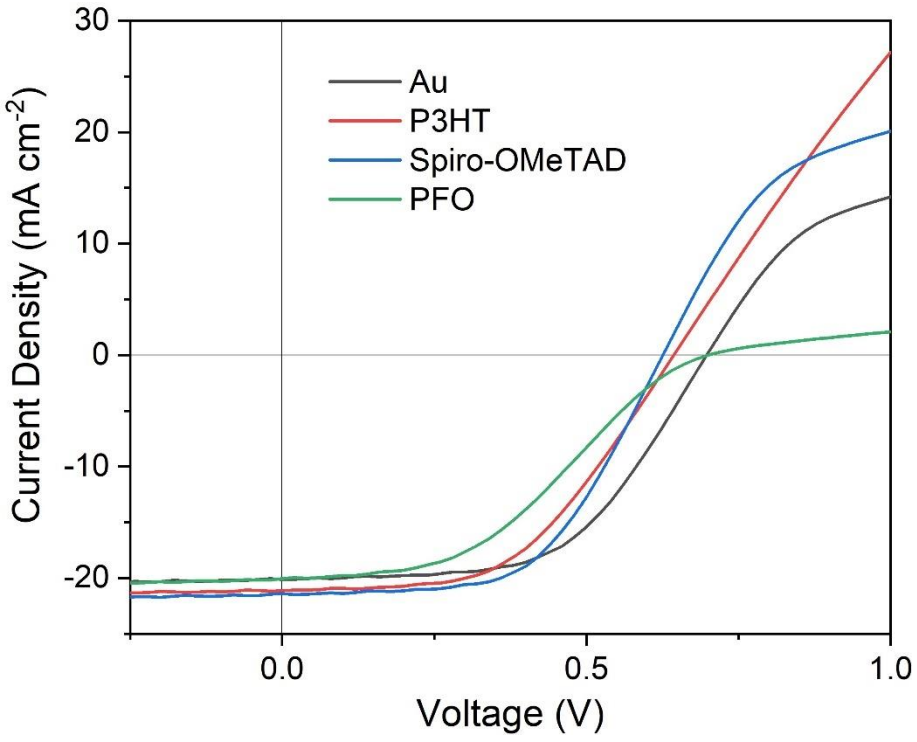

Figure 5.10: Light *JV* curves from the highest efficiency contact of devices with a P3HT, spiro-OMeTAD or PFO contact layer compared to a simple Au contact

The external quantum efficiency of the same devices is shown in Figure 5.11a, with the long wavelength region corresponding to the CdTe band gap cut-off shown at higher resolution being shown in Figure 5.11b. Both devices with a P3HT and spiro-OMeTAD contact layers show improved collection in the short wavelength region, which accounts for the improved J_{sc} measured for these devices compared to the control device. This improved blue response may be related to the extra anneal these devices received following deposition of the organic layers causing further oxidation of the CdS layer, which can be catalysed by the SnO_2 layer contact following chlorine treatment despite the relatively low temperatures involved [28]. In contrast, the quantum efficiency with a PFO layer is nearly identical to that of the simple Au contact across most of the spectrum and differs only in the long wavelength region where an additional shoulder of improved collection is observed. This additional response at long wavelength is found for all organic layers and has been reported previously for P3HT [9], reducing the minimum absorber band gap calculated from the intercept of the long wavelength linear region from 1.44 eV with a simple Au contact to 1.43 eV for devices with an organic contact. Considering the lack of interdiffusion observed during the 430°C chlorine treatment, it is unlikely the additional 150°C anneal these devices were subject to causes any further CdS_xTe_{1-x} formation thereby increasing long wavelength collect. Furthermore, the PFO device was not annealed yet shows the same long wavelength shoulder. Alternative explanations previously suggested include interface reflection or changes in back surface recombination [9].

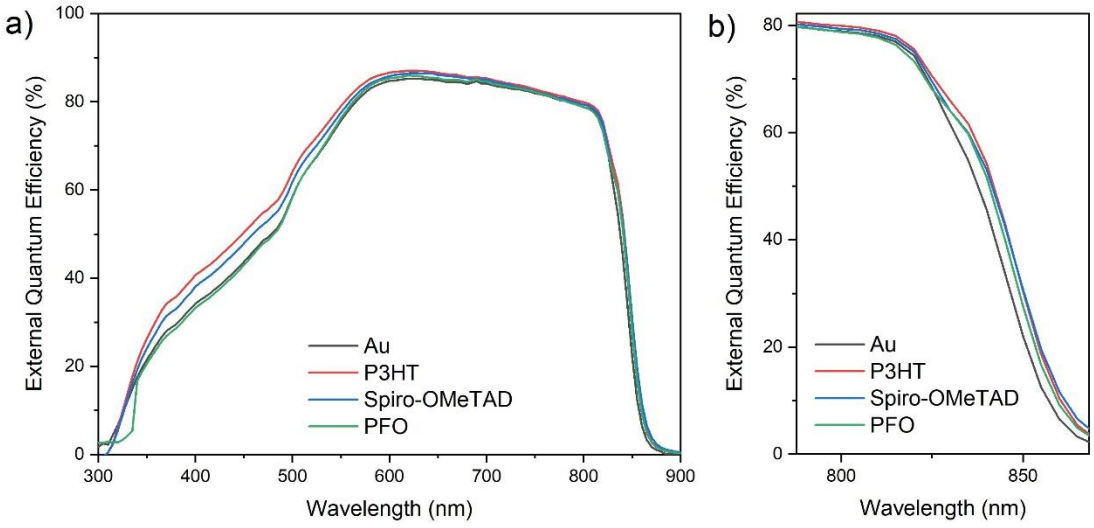

Figure 5.11: (a) External quantum efficiency of cells with highest efficiency from devices with P3HT, spiro-OMeTAD and PFO layers at the back contact compared to a simple Au contact, and (b) higher magnification view of the long wavelength region

CV profiling of these devices allows for the acceptor density as a function of depletion width to be determined via Mott-Schottky analysis (section 4.4.4), the results of which are shown in Figure 5.12. There is little change in the acceptor density between the devices with P3HT,

PFO and Au contacts which is to be expected since deposition of an additional interlayer at the back contact is unlikely alter the bulk properties of the CdTe absorber layer. However, in the case of devices with a spiro-OMeTAD layer there is a small but consistent upward shift of acceptor density profiles, indicating the CdTe layer in these devices has slightly higher *p*-type doping density concurrent with a small decrease in depletion width. Since the spiro-OMeTAD layer is doped with Li-TFSI, it is possible that lithium from the back contact has diffused into the CdTe layer during the post deposition annealing thereby increasing the doping density. Lithium is known to be an effective, albeit unstable, *p*-type dopant in CdTe single crystals which is highly mobile due to its small size [29]. Whilst there is only a minor increase in acceptor density evident from Figure 5.12, this characterizes the depletion region within the CdTe layer ~1 μm from the CdS interface, and it is therefore possible that the back contact region is more highly doped due to its close proximity to the lithium source, as well as having a tellurium rich composition arising from NP etching. This potential for localised doping at the back contact means it is difficult to disentangle the effect of the spiro-OMeTAD layer itself on device performance from potential *p*-type lithium doping of CdTe. Additionally, if lithium reaches the CdS layer it is expected to act as a compensating acceptor type defect, which would be detrimental to device performance and therefore further obscure the role of Li-TFSI addition. Further studies of the elemental composition throughout the CdTe device (e.g. SIMS measurements) would allow a clearer understanding of the changes in device performance with Li-TFSI doped spiro-OMeTAD layers.

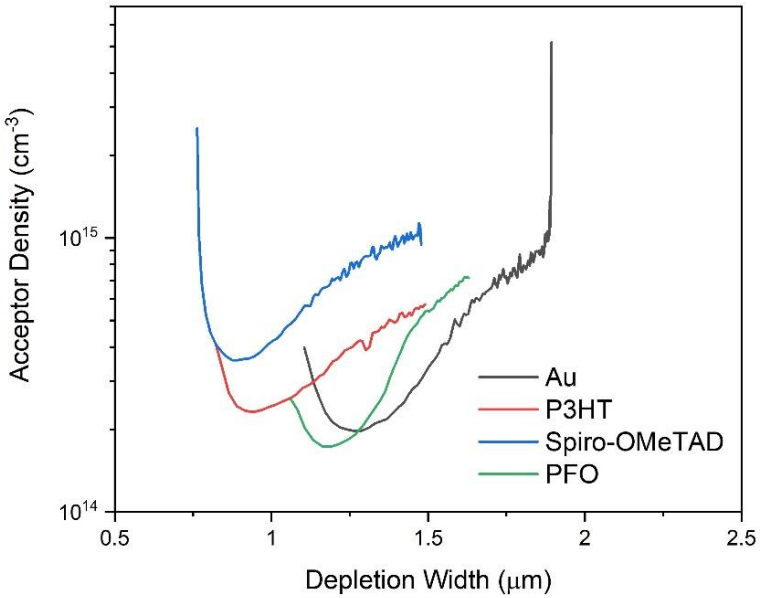

Figure 5.12: Net acceptor density profile taken from Mott-Schottky analysis of capacitance-voltage measurements of CdTe devices with P3HT, spiro-OMeTAD or PFO contact layers compared to device with a simple Au contact

The highest efficiency contact from each device was subject to temperature dependent *JV* measurements (section 4.4.2) between 200 – 300 K. This allows the ideality factor (n) and saturation current density (J_0) to be determined as a function of temperature which indicates the dominant current transport mechanism in the device, as well as the Schottky barrier height at the back contact indicated by the temperature dependence of series resistance. *JV* curves taken in the dark at temperatures between 200 – 300 K are shown in Figure 5.13 for each device. The semi log scale allows three distinct linear regions to be identified. Near short circuit, the ln(*J*) versus *V* response is flat with low current density that is insensitive to bias voltage. The intermediate region around 0.3 – 0.6 V in the semi log plots shows a linear region which corresponds to the exponential response of the main junction, and can be fit to the Schottky diode equation to find n and J_0. The curves then flatten again at higher forward bias as the back-contact diode begins to dominate, thereby limiting current density.

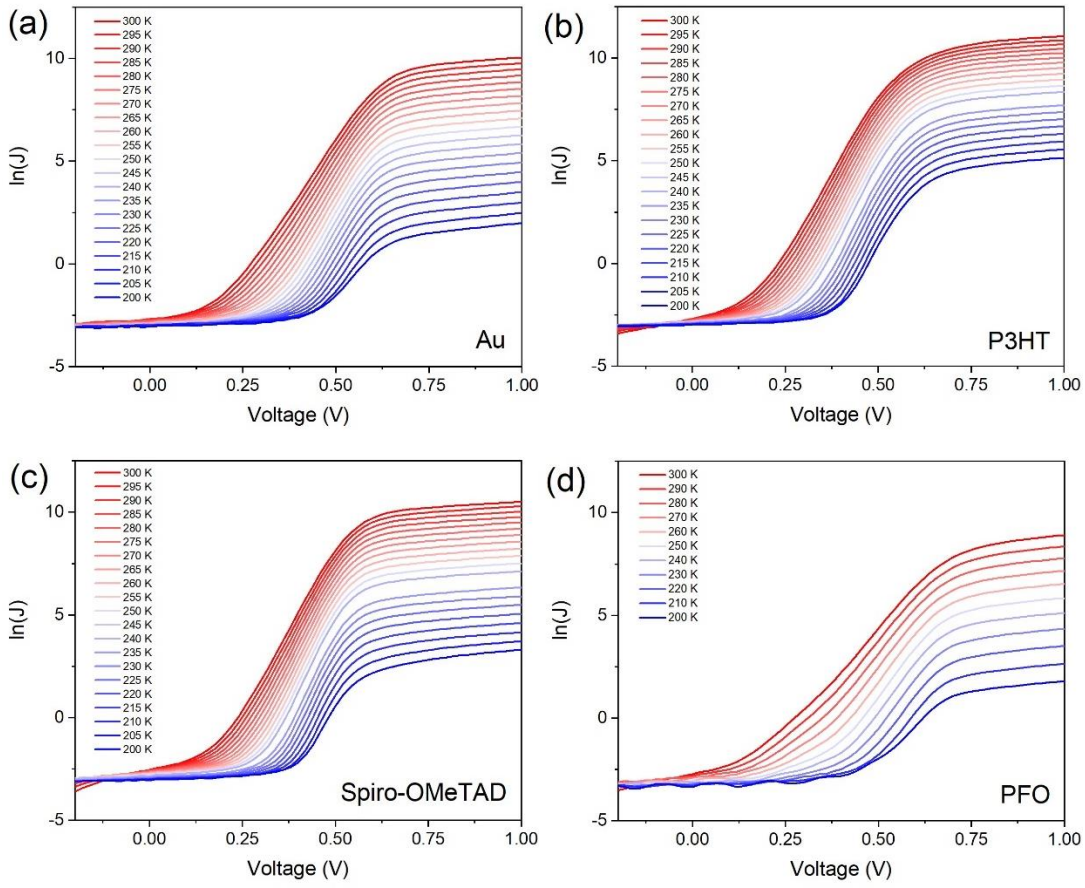

Figure 5.13: Dark *JV* measurements taken at temperatures between 200 – 300 K for CdTe devices with a standard Au contact (a) compared to devices with P3HT (b), spiro-OMeTAD (c) and PFO (d) layers between the CdTe and Au contact. The logarithm of current density is plotted to highlight the linear region which is used to determine the ideality factor and saturation current density.

Figure 5.14 shows the ideality factor and saturation current density of CdTe solar cells with different back contact structures, determined from the gradient and intercept of the linear

region of the main junction in semi log *JV* curves shown in Figure 5.13. As reviewed by Al Turkestani [30], the temperature dependence of n and J_0 can be used to identify current transport mechanisms in a solar cell. The data in Figure 5.14 broadly shows two regions whereby two different transport mechanisms dominate. At high temperatures (above ~250 K), the ideality factor does not vary significantly with temperature whilst the saturation current shows a $\ln J_0 \propto -1/T$ dependence. This is characteristic of carrier transport via a diffusion current ($n = 1$), recombination within the depletion region via mid gap trap states ($n = 2$) or some combination of the two ($1 < n < 2$). At lower temperatures, the ideality factor increases and $\ln J_0$ no longer shows a linear temperature dependence. This is characteristic of recombination via a multi-step tunnelling mechanism, whereby electrons and hole recombine by tunnelling through a series of closely spaced localised defect states. In this case the ideality factor has no physical meaning, especially above the limiting value of $n = 2$, however it is useful as a diagnostic tool to determine the transport mechanism. There is no sharp change in transport mechanism as observed by other authors [31]. Instead, a gradual transition between the two transport regimes is observed, with the transition temperature differing between devices.

In the high temperature regime, the ideality factor for devices with P3HT and spiro-OMeTAD interlayers is lower compared to the control device with a simple Au contact. This indicates an increase in the relative contribution of the diffusion current to carrier transport, whereas for PFO an ideality factor of ~1.8 suggests transport is largely dominated by SRH recombination. Although the incorporation of an additional layer at the back contact would be expected to have little impact on carrier transport across the CdS-CdTe junction, the efficiency of hole extraction and electron injection will likely be influenced by the position of the HOMO and LUMO level of the organic layers respectively. This could therefore alter the forward current density throughout the device and consequently on recombination dynamics within the depletion region. It should be noted that neither the observed ideality factor nor saturation current density correlate to the V_{oc} of devices shown in Figure 5.10. Although an ideality factor closer to 1 and low J_0 would be expected to lead to a high open circuit voltage, both the P3HT and spiro-OMeTAD devices have lower V_{oc} than the Au device. On the other hand, the PFO device has a much higher ideality factor and increased J_0 yet maintains the same V_{oc} as the control device.

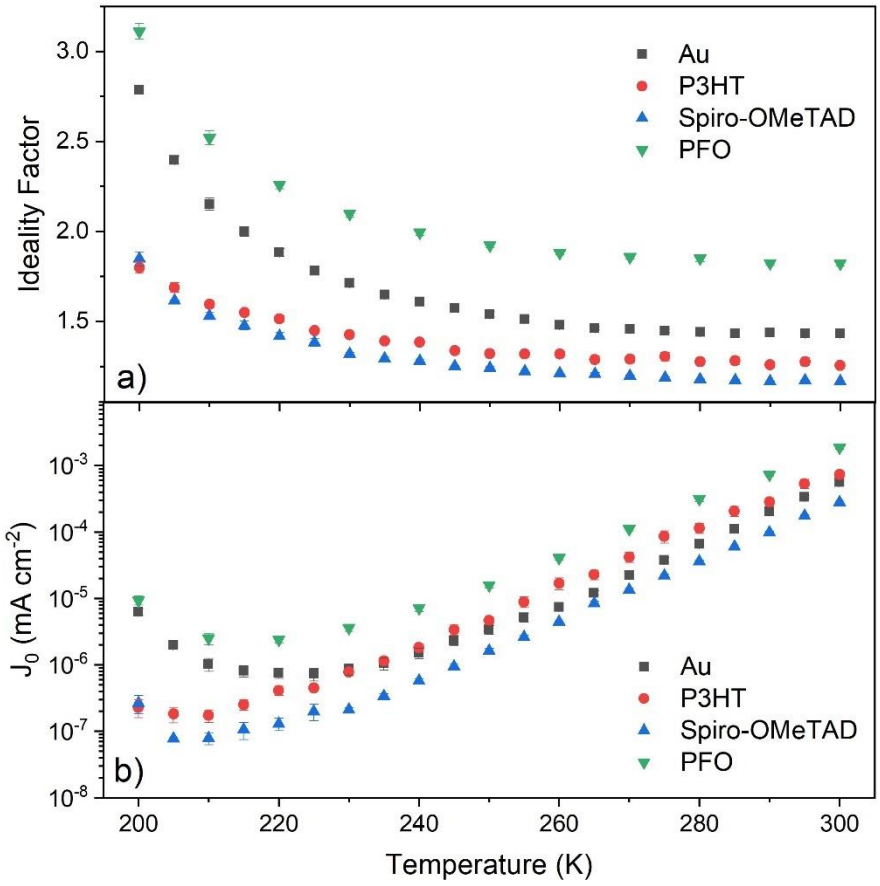

Figure 5.14: Temperature dependence of (a) ideality factor and (b) saturation current density, calculated from *JVT* measurements of CdTe solar cells with P3HT, spiro-OMeTAD and PFO back contacts compared to a Au-only contact

The series resistance of each of the devices was measured in forward bias before the onset of rollover, and is shown as a function of temperature in Figure 5.15. The Schottky barrier height at the back contact is determined for each device structure using the method outlined by Bätzner et al [32], and shows that all three of the organic contacts studied here are effective in lowering the back contact barrier height therefore aiding hole extraction. P3HT lowers the barrier height by ~0.1 eV compared to the Au only contact and results in a dramatic reduction in series resistance at low temperature. This is consistent with previous reports studying CdTe solar cells with P3HT contacts [9] as well as the reduced rollover observed in Figure 5.10. Spiro-OMeTAD leads to a more modest ~0.02 eV barrier height reduction and has higher absolute series resistance compared to P3HT despite Li-TFSI doping, although this remains substantially lower than for a simple Au contact. PFO lowers the barrier height by 0.09 eV compared to Au, which is not immediately obvious from Figure 5.15a since this is accompanied by an increased absolute series resistance. However, it can be seen in the normalised data shown in Figure 5.15b that it is the temperature dependence of series resistance, rather than its absolute value, that describes barrier height. The series resistance of

the overall device is increased despite the lower barrier height, presumably due to the high resistivity of the PFO layer itself.

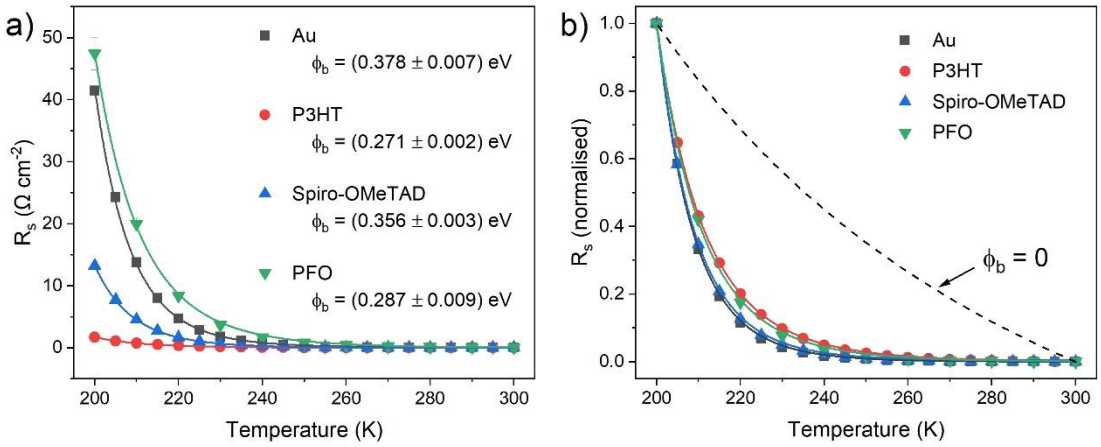

Figure 5.15: Temperature dependence of (a) raw and (b) normalised series resistance for different back contact structures, with the expected dependence in the limit of zero barrier height shown for reference. The barrier height is determined in each case following the method outlined by Bätzner et al [32]

Whilst all three organic contacts reduce the Schottky barrier height at the back contact of CdTe solar cells, P3HT and PFO are clearly more effective compared to spiro-OMeTAD. The mechanism behind this improvement remain unclear since the extent to which barrier height is lowered does not appear to directly correlate with the HOMO position of the organic layer. An intermediate HOMO position between the valence band of CdTe and the work function of Au (-6.1 eV and -5.1 eV respectively [9]) would presumably create a staggered band alignment and therefore allow optimum hole transfer [33]. However, P3HT and spiro-OMeTAD have similar HOMO positions of -5.1 eV and -5.2 eV respectively [9,17] yet the addition of P3HT yields a more ohmic contact. On the other hand, PFO has a higher HOMO position of -5.8 eV [17] yet results in a similar barrier height to P3HT.

Spiro-OMeTAD has previously been reported to improve the contact to nanocrystalline CdTe solar cells via an interfacial dipole effect [13]. PFO and P3HT may act in a similar manner, although the differences in work function, LUMO position, conductivity and interfacial defects means that the mechanism by which these organics lower barrier height cannot be determined. Further systematic study of the effect of each of these parameters may allow clearer insight into the effect of organic contacts and inform the design of better interlayers, with organic semiconductors offering an ideal platform with which to carry out such tests due to their highly controllable and tuneable nature.

5.3.4 Pinhole blocking

As well as finding use as hole transport materials for solar cells, organic semiconductor layers have also been investigated as potential pinhole blocking layers to improve the uniformity and repeatability of device performance. The addition of a moderately resistive organic layer at the back surface of CdTe devices can prevent areas of weak diode response due to pinholes by preventing direct contact between the front and back electrodes. In effect, they serve a similar role to that of highly resistive transparent (HRT) layers at the front contact [34], which prevent shunting pathways but can also modify the interfacial alignment to improve carrier extraction. This is especially relevant to thin film solar cells in the early stages of development for which poorly optimised processing parameters can lead to inhomogeneous films with a high pinhole density [35]. An effective pinhole blocking layer offers the potential for devices with thinner absorber layers, hence reducing materials usage whilst aiding carrier extraction. Both P3HT [9] and polyaniline [14] have previously been studied as pinhole blocking layers for CdTe and have showed promising results.

Given the indications in Figure 5.9 of clear differences in the number of shunted cells between device structures, a more thorough assessment of the pinhole blocking effectiveness of P3HT, spiro-OMeTAD and PFO is now presented in comparison to a simple Au contact. This analysis is performed on the same device series as described in section 5.3.2, with a 5×5 cm^2 sample processed for each contact structure resulting in 36 cells per device. For the device with a PFO contact, two cells were not covered completely by the organic layer and are therefore only 34 cells are reported in this case.

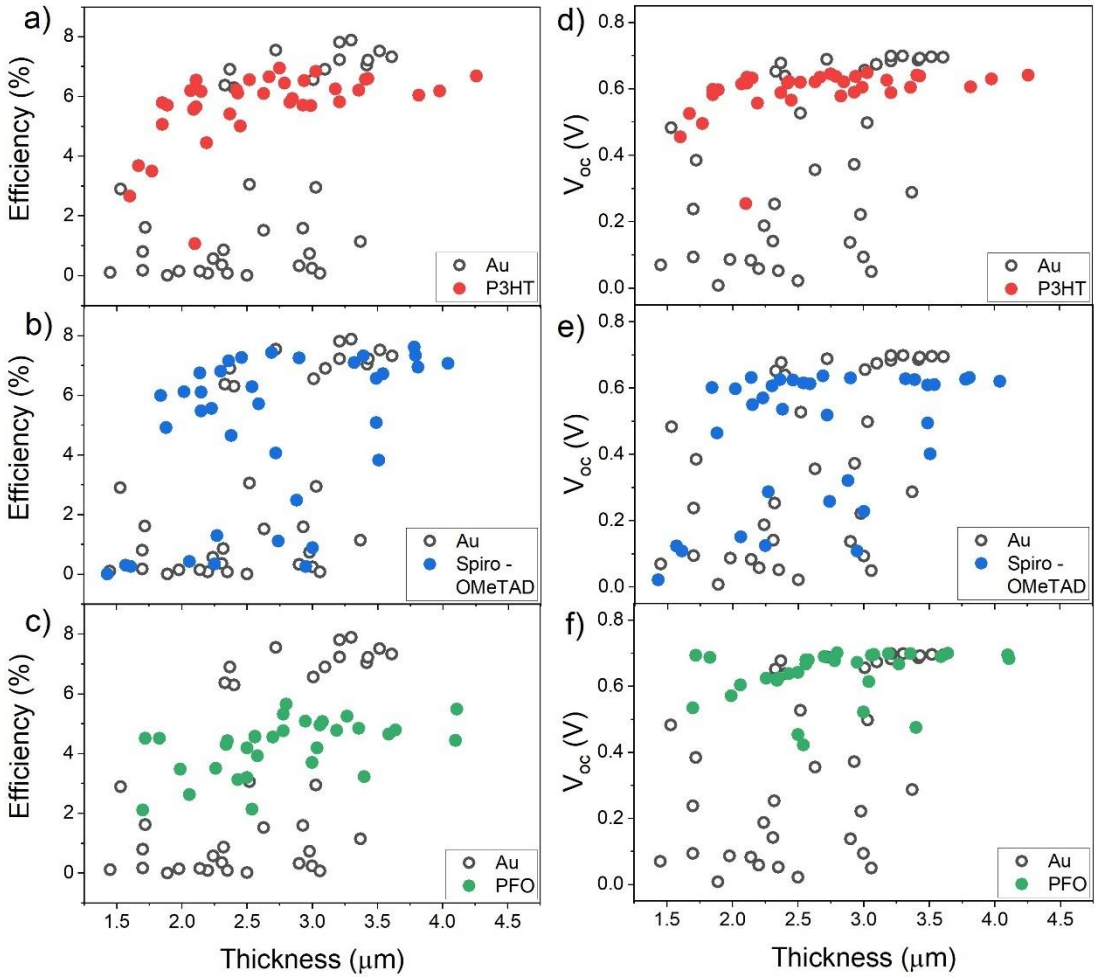

Figure 5.16: Efficiency and open circuit voltage as a function of CdTe thickness for devices with (a,d) P3HT, (b,e) spiro-OMeTAD, (c,f) PFO contacts compared to a device with a standard Au contact

Whilst the highly absorbing nature of CdTe means that ~2 μm is sufficient to capture the majority of above band gap photons, in practice it is challenging to deposit high quality layers at this thickness over a significant area and therefore thicker layers are typically used. CdTe devices grown at Liverpool typically require an absorber thickness of around 4 – 6 μm to ensure suitable coverage and repeatable performance. However, for this sample fabrication a thinner layer with a graded thickness between 1.5 – 4.5 μm was deposited by purposely changing the deposition geometry. The thickness of the absorber layer in each case was determined via profilometry by measuring across a scribe in the centre of the cell area following *JV* measurement. Figure 5.16 compares the efficiency and open circuit voltage of devices with different contact structures as a function of absorber layer thickness, with thinner layers anticipated to have a higher density of pinholes and hence areas with a weak diode response. The efficiency and open circuit voltage are presented for each device structure since they are strongly sensitive to the effect of pinholes, however the other performance parameters showed similar trends.

The same data series showing the performance of cells with Au contacts from a single device is presented in all graphs within Figure 5.16 to give a comparison with each organic contact. These Au-only cells display a wide variation in efficiency that is not strongly correlated with absorber thickness, instead showing two distinct groupings of datapoints with either typical efficiency around 6 – 8 %, or low efficiency around 0 – 2% whereby devices have either partially or entirely short circuited. The open circuit voltage, which is highly sensitive to the diode strength over a cell area, shows a more continuous distribution of intermediate values with a less clear distinction between 'working' and 'shunted' cells. The addition of a P3HT layer between the CdTe surface and Au contact results in a much more tightly distributed data series for both efficiency and V_{oc}. In comparison to the Au-only contact, none of these cells are entirely short circuited all demonstrate some level of photovoltaic response, with just one cell out of 36 showing significantly lower performance which is likely the result of a substantial pinhole. The efficiency and V_{oc} of devices show very little sensitivity to absorber layer thickness above 2 μm, which is a strong indication of pinhole blocking with P3HT which has been observed previously [9]. Cells with thinner absorber layers (below 2 μm) begin to show a decrease in efficiency, which is likely due to a combination of transmission losses [15] and the onset of a weakened diode response due to the inability of P3HT to entirely negate the harmful effect of pinholes. The addition of P3HT onto the back surface of these devices allows a clear trend of decreasing efficiency with reduced absorber thickness that is not apparent for devices with Au contacts.

The addition of spiro-OMeTAD at the back contact has a far lesser effect on the uniformity of the cell efficiency and V_{oc}, with several cells having low V_{oc} and efficiency at different thicknesses. Nonetheless, the average efficiency and V_{oc} are higher than that of the Au only device despite lower peak performance, suggesting some level of improved uniformity. PFO acts in a similar manner to P3HT in improving device uniformity and is especially effective in maintaining V_{oc} across all CdTe thicknesses with no shunted devices, whereas several Au-only cells show poor performance across a range of thicknesses. Again, the thinner absorber layers begin to show a decrease in V_{oc} suggesting a limit to the extent to which this pinhole-blocking strategy can be effective. The absolute efficiency of PFO devices is also below that of the 'working' Au-only cells and therefore the improved uniformity must be balanced with the increased resistivity of this device structure.

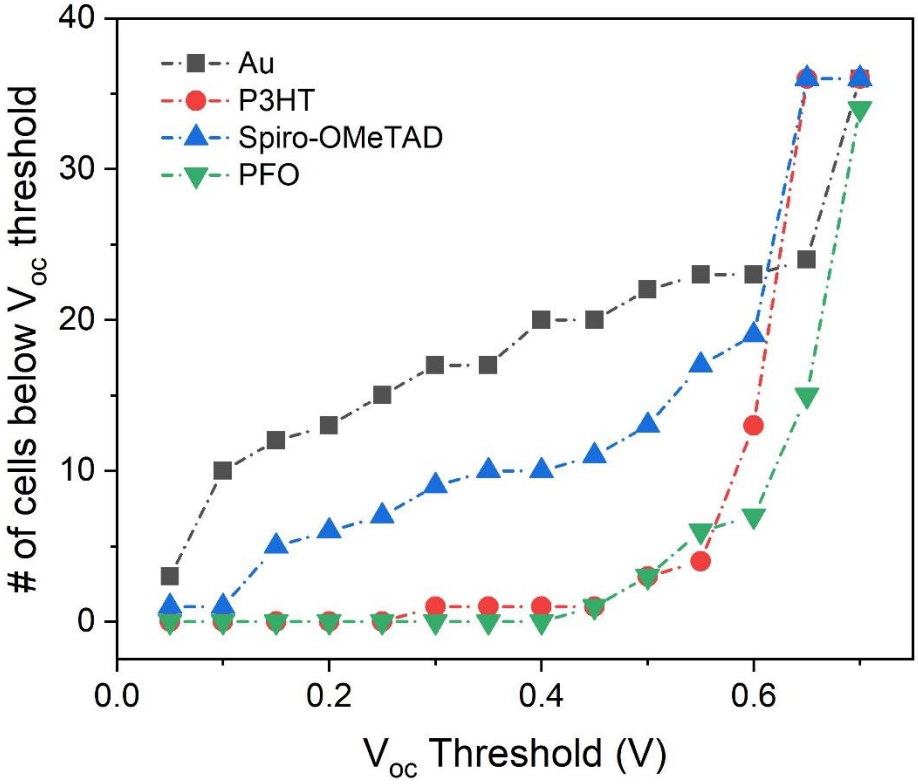

Figure 5.17: Number of cells with open circuit voltage below a varying threshold voltage for devices with organic back contacts compared to a standard Au contact.

Figure 5.17 shows the number of cells from each device where the V_{oc} falls below that of a V_{oc} threshold value. This allows a more quantitative comparison of the uniformity of the devices and therefore the ability of these organic layers to block pinholes to be assessed. V_{oc} is taken here as a proxy for junction quality, with low V_{oc} indicating a partially or entirely shunted cell. Ideally, all cells on an entirely uniform device would show identical performance and therefore have the same V_{oc}, which would result in a step function on a graph such as that in Figure 5.17. In reality, there is a distribution of voltages and therefore a more gradual, sloping curves which vary from one type of contact to another.

In Figure 5.17, the device with an Au contact does not show a sharp onset near its peak V_{oc} value, instead showing a gradual increase across all threshold voltages. This implies a non-uniform device performance which is easily observed from Figure 5.16 where several cells are clearly affected by pinholes. The addition of either P3HT or PFO drastically reduces the number of 'failed' cells across most threshold voltages, with almost all cells reaching V_{oc} above 0.5 V, before a rapid increase as threshold voltages close the maximum V_{oc} for each device. When plotted in this way it can be seen that both P3HT and PFO are equally effective in blocking pinholes, with the slightly earlier onset for the P3HT device due to the lower open circuit voltage for this device structure. It can be seen from Figure 5.16 that spiro-OMeTAD

has several shunted cells which are presumably caused by pinholes. However, Figure 5.17 shows that whilst not entirely effective in blocking pinholes, there are fewer 'failed' cells at each voltage threshold compared to the Au-only device. This indicates that the effectiveness of spiro-OMeTAD in pinhole blocking is intermediate between that of either P3HT or PFO and a standard Au contact, which is not immediately apparent from simply plotting efficiency or V_{oc} against absorber thickness. Since the spiro-OMeTAD was doped with Li-TFSI to increase its conductivity, this could explain why it is less effective in blocking pinholes. Further investigation into the relationship between the conductivity of such a pinhole blocking layer and the uniformity of device response would be beneficial.

5.4 Conclusions

Three organic semiconductors, P3HT, spiro-OMeTAD and PFO have been investigated as potential contacts for CdTe solar cells and compared to a standard Au-only contact. Thin films were spin coated onto the back surface of CdTe solar cells prior to metallization with Au. The performance of devices with P3HT and spiro-OMeTAD contacts was found to depend strongly on processing conditions, most notably post deposition annealing and doping. Incorporation of a PFO layer on the other hand always resulted in low efficiency devices regardless of how the devices were prepared due to its high resistivity.

After optimisation of deposition conditions, each of the organic contact layers were compared against a simple Au contact that had been applied directly to the CdTe surface. Devices with P3HT and spiro-OMeTAD layers showed higher J_{sc} but lower V_{oc} leading to a slight reduction in efficiency compared to a standard Au device, although further optimisation may be expected to overcome this [9,13]. Devices with a PFO layer maintained the same J_{sc} and V_{oc} as the control device, but a had a significantly lower fill factor due to increased series resistance. All of the organic contacts resulted in a reduced Schottky barrier at the back contact which is favourable for efficient hole extraction. Both P3HT and PFO were found to be particularly effective at lowering the barrier height, despite a significant difference in HOMO position and therefore dissimilar band alignments at the back contact.

Since the lower barrier height achieved were reliant on the introduction of an extra layer which therefore increased series resistance, the lower peak conversion efficiencies are unsurprising. Despite this, the *average* efficiency of each of the devices with organic contact layers was higher than the control device with a simple Au contact. The principal benefit of these organic

contact structures is the improved uniformity of performance due to a pinhole blocking effect. To test this, devices were grown with an intentional thickness variation of the CdTe layer. Regions of the device with a thinner absorber layer are especially prone to pinhole related losses, particularly in the case of large grained material grown by CSS. Whilst the Au-only device showed a large amount of variability with no clear dependence on absorber thickness, the addition of P3HT or PFO results in tightly distributed performance parameters that allows easy identification of trends within the data. Spiro-OMeTAD was partially effective in blocking pinholes since less cells were either partially or entirely shunted, although the effect was demonstrably less than either P3HT or PFO.

Whilst this work demonstrates some of the potential of organic layers in CdTe solar cells and for inorganic PV in general, the enormous scope of possibilities opened up by organic chemistry means that this barely scratches the surface of possibilities of a combined organic-inorganic structure. For this work, a set of candidate materials with promising properties were identified and deposition processes developed for each. Because this investigation has studied three different organic materials, each with different band structures, conductivities, and processing requirements, this makes meaningful comparisons of their precise effects on device performance challenging. Follow up studies may focus on, for example, the effect of systematically varying the HOMO position of the organic layer on contact barrier height and therefore hole extraction. This could be feasible through the appropriate choice of organic compound and functional groups, though will still involve a significant amount of development work. The effect of conductivity of an organic layer is important in determining its effectiveness in aiding hole extraction, but also on its ability to effectively block pinholes. This also warrants further investigation through molecular doping and is likely to be balanced with a requirement for minimising overall series resistance.

5.5 References

1. Geisthardt, R. M., Topič, M. & Sites, J. R. Status and potential of CdTe solar-cell efficiency. *IEEE J. Photovoltaics* **5**, 1217–1221 (2015).
2. Fahrenbruch, A. L. Ohmic contacts and doping of CdTe. *Sol. Cells* **21**, 399–412 (1987).
3. Demtsu, S. H., Albin, D. S., Sites, J. R., Metzger, W. K. & Duda, A. Cu-related recombination in CdS/CdTe solar cells. *Thin Solid Films* **516**, 2251–2254 (2008).
4. Li, X., Niles, D. W., Hasoon, F. S., Matson, R. J. & Sheldon, P. Effect of nitric-phosphoric acid etches on material properties and back-contact formation of CdTe-based solar cells. *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.* **17**, 805 (1999).
5. Rioux, D., Niles, D. W. & Höchst, H. ZnTe: A potential interlayer to form low resistance back contacts in CdS/CdTe solar cells. *J. Appl. Phys.* **73**, 8381 (1993).
6. Xia, W. *et al.* Te/Cu bi-layer: A low-resistance back contact buffer for thin film CdS/CdTe solar cells. *Sol. Energy Mater. Sol. Cells* **128**, 411–420 (2014).
7. Hu, S. *et al.* Band diagrams and performance of CdTe solar cells with a Sb_2Te_3 back contact buffer layer. *AIP Adv.* **1**, 042152 (2011).
8. Lin, H., Xia, W., Wu, H. N. & Tang, C. W. CdS/CdTe solar cells with MoO_x as back contact buffers. *Appl. Phys. Lett.* **97**, 123504–2881 (2010).
9. Major, J. D. *et al.* P3HT as a pinhole blocking back contact for CdTe thin film solar cells. *Sol. Energy Mater. Sol. Cells* **172**, 1–10 (2017).
10. Jarkov, A. *et al.* Conductive polymer PEDOT:PSS back contact for CdTe solar cell. *Thin Solid Films* **519**, 7449–7452 (2011).
11. Wang, W., Paudel, N. R., Yan, Y., Duarte, F. & Mount, M. PEDOT:PSS as back contact for CdTe solar cells and the effect of PEDOT:PSS conductivity on device performance. *J. Mater. Sci. Mater. Electron.* **27**, 1057–1061 (2016).
12. Walkons, C., Guralnick, B., McCandless, B. & Birkmire, R. CdTe solar cells with a PCBM back contact. in *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)* 1567–1572 (IEEE, 2014). doi:10.1109/PVSC.2014.6925217
13. Du, X. *et al.* Improvement in open-circuit voltage of thin film solar cells from aqueous nanocrystals by interface engineering. *ACS Appl. Mater. Interfaces* **8**, 900–907 (2016).
14. Tessema, M. M. & Giolando, D. M. Pinhole treatment of a CdTe photovoltaic device by electrochemical polymerization technique. *Sol. Energy Mater. Sol. Cells* **107**, 9–12 (2012).
15. Paudel, N. R., Wieland, K. A. & Compaan, A. D. Ultrathin CdS/CdTe solar cells by sputtering. *Sol. Energy Mater. Sol. Cells* **105**, 109–112 (2012).
16. Rockett, A. Organic Semiconductors. in *The Materials Science of Semiconductors* 395–453 (Springer US, 2008). doi:10.1007/978-0-387-68650-9_9
17. Zhu, Z. *et al.* Polyfluorene derivatives are high-performance organic hole-transporting materials for inorganic-organic hybrid perovskite solar cells. *Adv. Funct. Mater.* **24**, 7357–7365 (2014).

18. Kanai, K. *et al.* Effect of annealing on the electronic structure of poly(3-hexylthiophene) thin film. *Phys. Chem. Chem. Phys.* **12**, 273–282 (2010).

19. An, L., Duan, Y., Yuan, Y., Zhou, L. & Zhang, J. Effect of thermal annealing on the microstructure of P3HT thin film investigated by RAIR spectroscopy. *Vib. Spectrosc.* **68**, 40–44 (2013).

20. Cappel, U. B., Daeneke, T. & Bach, U. Oxygen-induced doping of spiro-MeOTAD in solid-state dye-sensitized solar cells and its impact on device performance. *Nano Lett.* **12**, 4925–4931 (2012).

21. Wang, S. *et al.* Role of 4-tert-butylpyridine as a hole transport layer morphological controller in perovskite solar cells. *Nano Lett.* **16**, 5594–5600 (2016).

22. Mariotti, S. *et al.* Stability and performance of $CsPbI_2Br$ thin films and solar cell devices. *ACS Appl. Mater. Interfaces* **10**, 3750–3760 (2018).

23. Pellaroque, A. *et al.* Efficient and stable perovskite solar cells using molybdenum tris(dithiolene)s as p-dopants for spiro-OMeTAD. *ACS Energy Lett.* **2**, 2044–2050 (2017).

24. Wang, X., Sarvari, H., Dang, H., Chen, Z. & Singh, V. Evolution characteristics of perovskite solar cells in air and vacuum environments. *Optik (Stuttg).* **150**, 111–116 (2017).

25. Hu, J. *et al.* Polyfluorene copolymers as high-performance hole-transport materials for inverted perovskite solar cells. *Sol. RRL* **4**, 1900384 (2020).

26. Sekine, C., Tsubata, Y., Yamada, T., Kitano, M. & Doi, S. Recent progress of high performance polymer OLED and OPV materials for organic printed electronics. *Sci. Technol. Adv. Mater.* **15**, (2014).

27. Hwang, J. & Kahn, A. Electrical doping of poly(9,9-dioctylfluorenyl-2,7-diyl) with tetrafluorotetracyanoquinodimethane by solution method. *J. Appl. Phys.* **97**, 103705 (2005).

28. Perkins, C. L., McGott, D. L., Reese, M. O. & Metzger, W. K. SnO_2-catalyzed oxidation in high-efficiency CdTe solar cells. *ACS Appl. Mater. Interfaces* **11**, 13003–13010 (2019).

29. Crowder, B. L. & Hammer, W. N. Shallow acceptor states in ZnTe and CdTe. *Phys. Rev.* **150**, 541–545 (1966).

30. Al Turkestani, M. K. CdTe solar cells: Key layers and electrical effects. (2010).

31. Williams, B. L. CdTe nanowire structures for solar cells. (2013).

32. Bätzner, D. L., Öszan, M. E., Bonnet, D. & Bücher, K. Device analysis methods for physical cell parameters of CdTe/CdS solar cells. *Thin Solid Films* **361**, 288–292 (2000).

33. Bhandari, K. P. *et al.* Very high V_{oc} and FF of CdTe thin-film solar cells with the applications of organo-metallic halide perovskite thin film as a hole transport layer. *Prog. Photovoltaics Res. Appl.* pip.3309 (2020). doi:10.1002/pip.3309

34. McCandless, B. E. & Dobson, K. D. Processing options for CdTe thin film solar cells. *Sol. Energy* **77**, 839–856 (2004).

35. Kaienburg, P. *et al.* How contact layers control shunting losses from pinholes in thin-film solar cells. *J. Phys. Chem. C* **122**, 27263–27272 (2018).

Chapter 6

Incorporation of sodium into CdTe solar cells

Part of this chapter is based on work that has previously been published as:

T. P. Shalvey and J. D. Major, "Impact of NaF during chloride treatment of CdTe solar cells", Materials Science in Semiconductor Processing (2020), ***107*** *104827*

6.1 Introduction

The impact of sodium incorporation in CdTe solar cells is important to understand due to the large Na content of soda-lime glass (around 15% Na_2O by weight [1]). These alkali containing substrates are cheaper to produce and therefore necessary in the low cost, high throughput manufacturing processes used for commercial modules to remain competitive. Whilst barrier layers such as SiO_2 are typically used to prevent out diffusion [2], they are not fully effective given the high temperature processing conditions used [3] and therefore it is inevitable that some sodium ends up in the active layers of the device. Even in trace quantities this can have significant impact on the optoelectronic properties of CdTe and therefore on device performance [4,5].

Sodium is expected to be a *p*-type dopant with a shallow Na_{Cd} acceptor level 59 meV from the valence band [6], compared to the much deeper 160 meV for Cu_{Cd} meaning Na is more favourable for achieving high doping densities. The interstitial Na_i donor level is similarly shallow from the conduction band and therefore is not expected to severely reduce carrier lifetime, however if present in significant quantities it will cause carrier compensation and limit achievable doping densities, meaning careful process control is required.

Previous attempts to incorporate sodium into CdTe solar cells have focused mainly on the use of NaF [4,7,8], which is commonly used in high efficiency CIGS devices. In all prior reports,

sodium deposition was carried out prior to chlorine activation meaning the NaF treatment was performed at the $CdCl_2$ processing temperature, typically > 400°C. Whilst some increase in doping density was observed, it was accompanied by significant structural changes, with enhanced recrystallization leading to widened grain boundaries and poor quality junctions that ultimately reduced device performance. This work attempts to retain the beneficial effects observed by some authors following NaF treatment, whilst avoiding the detrimental structural changes. One approach is to separate the doping process from the recrystallization by depositing NaF after $MgCl_2$ treatment, thereby allowing the sodium treatment to be performed at lower temperature than required for chlorine activation. Alternatively, a combined NaF and $MgCl_2$ treatment is investigated for large grain CdTe material which is less prone to recrystallisation, and combined with a more robust SnO_2 window layer in place of CdS to prevent excessive interdiffusion.

6.2 Sodium doping of CdTe via evaporation of NaF layers post $MgCl_2$ treatment

Previous attempts to incorporate sodium into CdTe devices via NaF deposition have been hindered by deleterious structural changes caused by aggressive recrystallization. However, these approaches have focused on the deposition of the NaF layer prior to the chlorine activation step, and therefore it is subject to high temperatures (> 400°C) and offers little control of what is likely a very mobile species in CdTe. By separating the chlorine activation from the NaF processing step, it may be possible to control the doping process more precisely and avoid the adverse structural changes such as widened gain boundaries and window layer agglomeration.

6.2.1 Device fabrication

A series of 8 devices were made by sputtering CdS onto TEC15M substrates, followed by close spaced sublimation of 5 – 6 μm CdTe in 30 Torr N_2 (T_{source} = 610°C, $T_{substrate}$ = 520°C). After a 15 second NP etch, samples were treated with $MgCl_2$ at 410°C for 20 min, left to cool to room temperature and were subject to a further 15 second NP etch. At this point, all devices had been fabricated in an identical manner. Following secondary NP etching, a control device was fabricated with a simple 50 nm Au back contact via thermal evaporation. For all other devices, 1 nm NaF was thermally evaporated onto the back surface. One device was left unannealed and the remaining six were annealed in air for 20 min at temperatures between

100 – 350°C, followed by the application of a 50 nm Au contact. Evaporation of NaF was initially complicated by its hygroscopic nature leading to unreliable thickness measurements on the QCM. This was overcome by gently preheating the source material at low temperature prior to the main deposition to remove any moisture, after which the evaporation rate is more constant.

A further device series was fabricated for further characterisation in a similar manner to that described above. In this set, a control device with a simple Au contact was compared with a device with 5 nm NaF deposited onto the etched back surface of a CdTe device and subsequently annealed at temperatures up to 300°C, instead of 1 nm to exaggerate any effect of the NaF treatment.

6.2.2 Effect of 1 nm NaF treatment temperature on device performance

Figure 6.1 shows *JV* curves from the highest efficiency cell of each of the devices with 1 nm NaF at the back surface subject to different anneal conditions compared to a control device without NaF. There is little difference between the shape of curves corresponding to the NaF treated devices, although the device annealed at 350°C shows noticeably poorer performance. Since it is difficult to observe trends directly from these *JV* curves, a more detailed discussion of the effect of anneal temperature on device performance is deferred to follow Figure 6.2. However, there are some obvious differences in the shape of *JV* curves with and without NaF treatment, regardless of the annealing temperature. Most notably, there is a striking difference between the shape of the curves in forward bias. The control device shows rollover above V_{oc}, which characteristic of a secondary barrier at the back contact. In contrast, all devices with NaF applied at back contact do not show such behaviour regardless of whether they are annealed or not, which suggests these devices have a reduced Schottky barrier. There is also a lower series resistance for NaF treated devices which can be observed from a steeper gradient around V_{oc} leading to an improved fill factor and is consistent with a lower contact barrier.

This improvement in contacting is presumably due to a highly doped back surface which results in a narrower barrier through which carriers can tunnel through to be extracted. In this case it is unsurprising that the doping of the back contact is less dependent on anneal temperature, since this would not require driving the sodium into the bulk of the device at an elevated temperature and the Te rich region formed at the back surface during etching means there are plenty of available Cd site to form Na_{Cd} acceptors. A similar strategy is commonly employed for copper doping in CdTe, whereby the back contact region is highly doped to form a p^+ region to assist the formation of an ohmic contact [9]. Replacing the copper at the back contact with a different *p*-type dopant such as sodium is highly desirable, since copper can

also incorporate on interstitial sites and form deep level defects in CdTe which are detrimental to device performance [10]. On the other hand, sodium interstitials are predicted to be much shallower and therefore whilst they are ideally avoided entirely since they compensate *p*-type doping, they are not expected to act as strong recombination centres and therefore will be less harmful [6]. The reduced rollover shown in Figure 6.1 following NaF treatment is therefore encouraging as this shows potential as a copper-free contact to CdTe. The long-term stability of NaF treated devices compared to a more typical Cu treatment, which is known to present degradation issues [11], is worthy of further investigation.

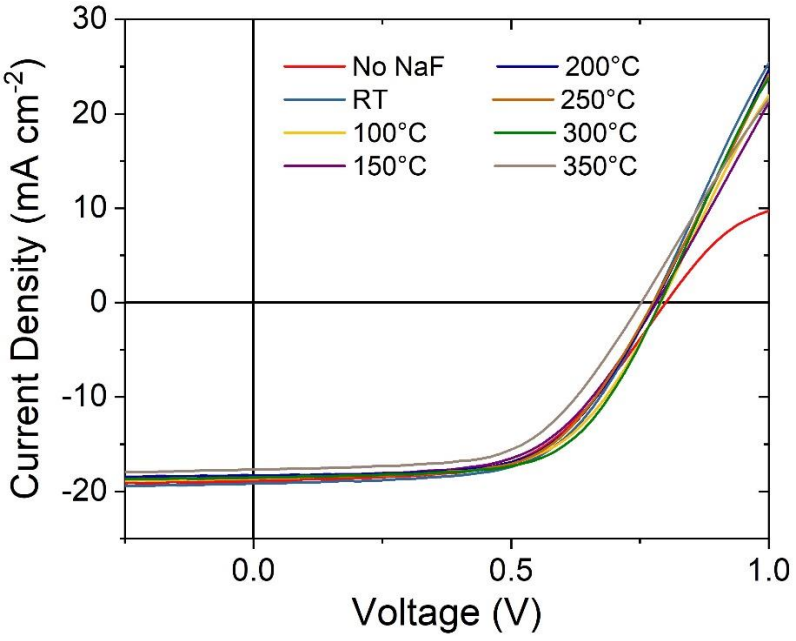

Figure 6.1: *JV* curves for the highest efficiency cell from devices with 1 nm NaF deposited prior to contacting annealed for 20 min at temperatures up to 350°C compared to a device without NaF

Figure 6.2 shows the average performance parameters as well as those of the highest efficiency cell for devices with 1 nm NaF as a function of annealing temperature compared to a control device without NaF. For all devices with NaF there is a decrease in both the average and peak V_{oc} and J_{sc} with increasing annealing temperature. However, there does appear to be a small reversal of this trend around 300°C that is especially visible in the highest efficiency cell series. In contrast, the fill factor tends to be increased for those devices containing NaF. This can mainly be attributed to a reduction in the series resistance of devices with NaF compared to the control device. This is most apparent for the un-annealed device but is evident for all NaF treatments, since the series resistance of the best cell remains lower in all cases than the control device, albeit with more variation with higher anneal temperatures. The shunt resistance appears to initially increase before peaking before around 200°C, and although increased shunt resistance will lead to a higher fill factor, the increase in this device series is dominated by the lower series resistance. The combined effect of all these parameter changes

with temperature means there is little overall change in the efficiency. Some of the higher temperature anneal devices suffered from several 'shunted' cells, which lowers the average efficiency, however in general the peak efficiency of cells tends to be slightly increased for most anneal temperatures, especially at 300°C.

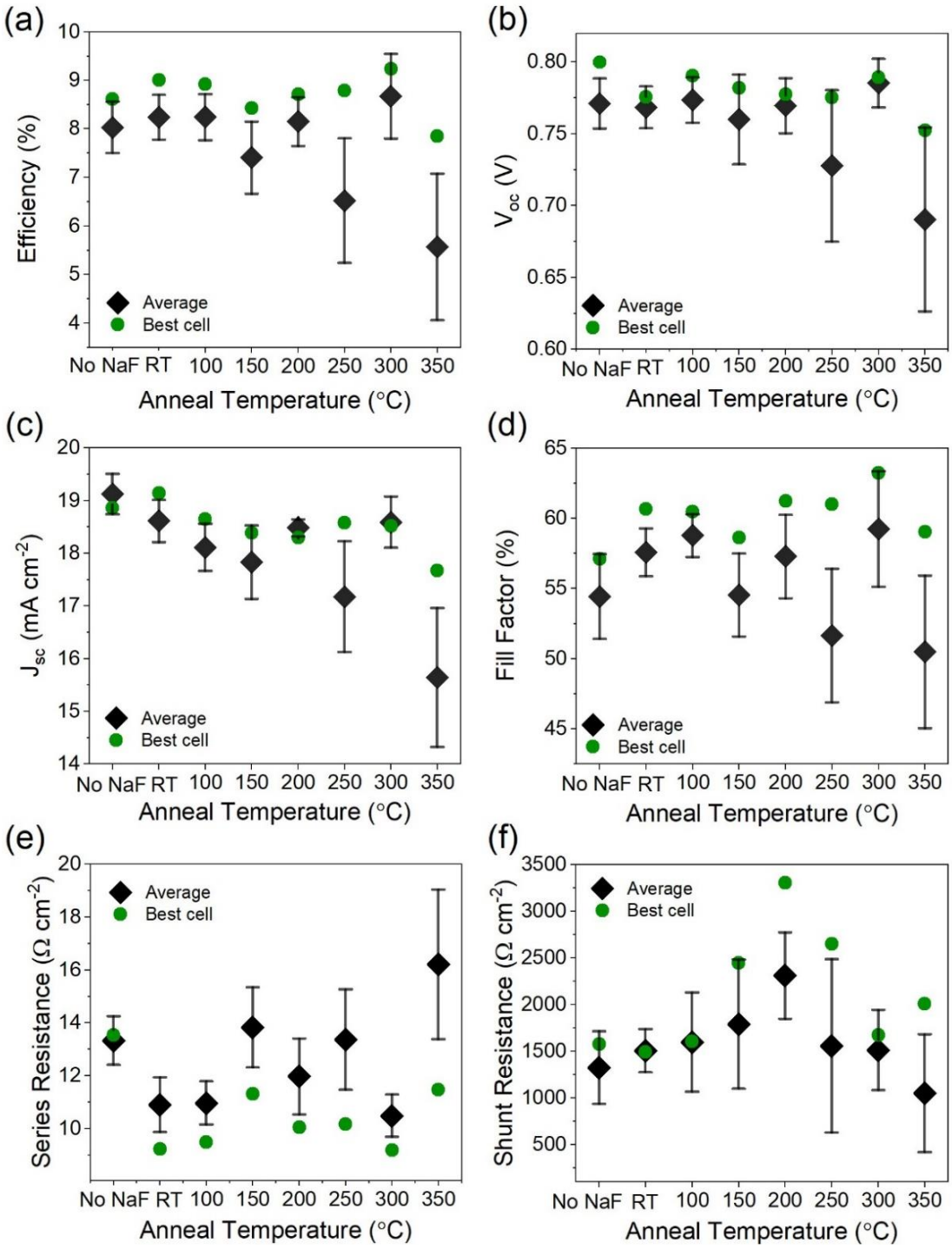

Figure 6.2: *JV* parameters showing (a) efficiency, (b) open circuit voltage, (c) short circuit current density, (d) fill factor, (e) series resistance and (f) shunt resistance of devices with 1 nm NaF evaporated prior to contacting and annealed for 20 min at various temperatures. Average values are shown with error bars corresponding to the standard deviation from nine 0.25 cm^2 cells per device, as well as the parameters for the highest efficiency cell from each device.

Clearly the data is heavily scattered, which limits the conclusions that can be drawn from this data series alone. This may be small due to inconsistencies in device processing and variations in thickness leading to pinholes etc, but also likely due to several overlapping processes occurring when NaF is deposited and annealed into the cell, for example oxidation of films as they are annealed whilst also redistributing NaF. However, it is clear that the addition of NaF is not causing a drastic reduction in device efficiency as seen by previous authors [4].

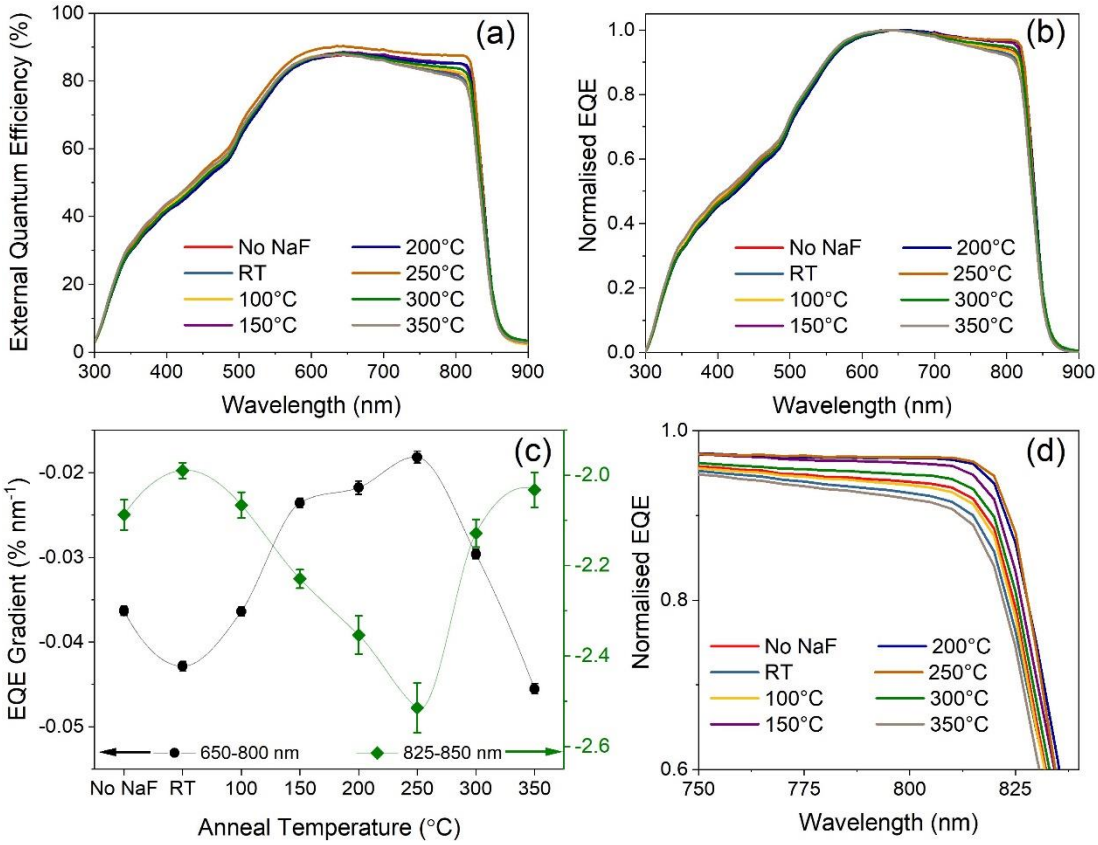

Figure 6.3: (a) Raw and (b) normalised EQE curves for champion cells from devices with 1nm NaF deposited prior to contacting and annealed up to 350°C, compared to a control device without NaF. (c) shows the gradient of the curves at long wavelength corresponding to the flat top and bandgap cut-off, representing the 'squareness' in this region with lines connecting datapoints shows as a guide to the eye. (d) shows the long wavelength region between 750-840 nm in more detail.

Figure 6.3 shows external quantum efficiency data for the highest efficiency cells from the NaF treated devices described previously. The EQE curves shown in Figure 6.3a are normalised to maximum collection efficiency for ease of comparison in Figure 6.3b, and show very little difference in the CdS shoulder region at short wavelength. In previous attempts to incorporate sodium into CdS/CdTe devices there has been significant recrystallization at the interface [4,5], consuming the CdS layer which manifests itself as an increase of EQE in the short wavelength region. Since there is no such effect observed here, it is likely that the CdS layer

remains intact and therefore can create a suitable junction with CdTe which can effectively separate charge carriers.

The long wavelength region of the normalised EQE curves shows a subtle trend with anneal temperature. This can be seen more clearly in Figure 6.3d which focuses on the shoulder region whereby collection efficiency decreases as the photon energy decreases below that of the CdTe band gap. To show the effect of NaF treatment on this long wavelength region more clearly, Figure 6.3c plots the gradient along the top of the normalised EQE curves between 650-800 nm, and the gradient corresponding to the CdTe bandgap cut-off between 825-850nm, as a function of NaF anneal temperature. Together these values give an indication of the 'squareness' of the EQE response at long wavelengths which corresponds to how well carriers are separated from deeper in the CdTe layer. With increasing anneal temperature, the top of the EQE curves become flatter (ie 650-800 nm gradient is less negative), whilst the CdTe bandgap cut-off becomes steeper (825-850 nm gradient is more negative). This means there is more efficient collection at long wavelength with increasing anneal temperature up to 250°C, where the trend is then reversed. This could result from a number of changes in the device, but given the results from capacitance-voltage measurements shown in Figure 6.4, this is likely caused by a changes in depletion width allowing more efficient collection further into the CdTe layer.

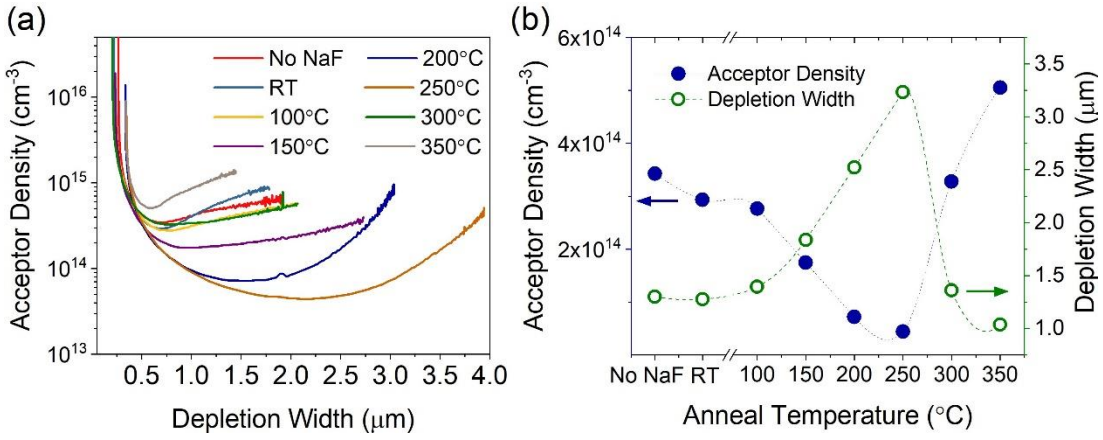

Figure 6.4: (a) acceptor density versus depletion width extracted from Mott-Schottky plots for devices with 1nm NaF annealed up to 350°C compared to a device without NaF, and (b) shows the bulk acceptor density taken from the minimum of these curves, as well as the depletion width at zero bias

Capacitance voltage measurements were performed on the best performing cell on each device, from which the doping density as a function of depletion width can be determined as shown in Figure 6.4a. There is clearly a change in both doping density and depletion width with varied annealing temperature, which can be seen clearer in Figure 6.4b, showing the acceptor density as measured from the minima of each curve, and the depletion width measured at 0 V bias. With the addition of NaF at the back surface and subsequently annealing

at temperatures up to 250°C there is a decrease in the bulk acceptor concentration, which implies that rather than forming acceptor levels by occupying Cd sites, it is instead forming compensating defects that act to reduce the overall doping density, likely by incorporating interstitially into the CdTe lattice. Above 250°C there is a sharp reversal of this trend with the acceptor concentration increasing with anneal temperature, reaching a maximum of a ~50% increase compared to the control device without NaF. At this temperature, it appears the incorporation onto Na_{Cd} sites is energetically favourable compared to Na_i incorporation, thereby increasing the doping density. Since the maximum temperature used in this study was limited to 350°C it remains unclear whether higher temperatures would facilitate higher doping densities, with preliminary test devices showing reduced performance due to the presence of a heavily oxidised back surface that accompanies the higher temperature anneals. The depletion width varies inversely with acceptor concentration, since lower doping density requires a larger volume of CdTe to balance the overall charge. The change in depletion width with anneal temperature can be seen to roughly match the trend in Figure 6.3b which can explain the improvement in EQE response at long wavelengths up to 250°C. Devices which have the largest depletion width allow more efficient collection of carriers further into the device, which long wavelength photons are more likely to reach. Since depletion width scales inversely with acceptor concentration, it is necessary to find a balance between a highly doped absorber to increase V_{oc}, whilst maintaining a sufficient electric field in the bulk of the device. That balance is typically around 10^{16} cm^{-3} for CdTe [12], much higher than observed here and therefore despite the reduced depletion width, annealing devices with NaF above 300°C is likely necessary for effective doping. However, the initial analysis shown here implies that this may not necessarily translate to higher efficiency due to secondary effects such as oxidation of the back surface and sodium accumulation in the CdS layer as discussed next.

6.2.3 SIMS and XPS analysis

Having looked at how annealing NaF affects CdTe at a device level, a more detailed study of the effects on the distribution of elements throughout the material was undertaken, as well as how this affected the quality of the CdTe absorber. It has been shown that the anneal temperature strongly influences the sodium incorporation into the device, with temperatures above 300°C required to increase the carrier concentration. Here a control device without NaF or annealing will be compared to devices with 1 nm NaF annealed in air at either low (200°C) or high (300°C) temperature.

Figure 6.5 shows the distribution of sodium, fluorine and chlorine measured via ToF-SIMS analysis and quantified by comparing these devices to ion-implanted reference standards for

each element in CdTe. Sodium is present in significant quantities in the control device without the intentional addition of NaF. There are several potential sources of Na, however, the concentration of ~10^{17} cm^{-3} in the bulk of the CdTe layer is consistent with previous reports where it is attributed to out-diffusion form the glass substrate [13–15]. Furthermore, ICP-OES measurements of new CdTe source material (Alfa Aesar, 5N) shows Na to be present in a concentration of (4.2 ± 0.2) × 10^{17} cm^{-3} before being loaded into the CSS chamber, which could also account for the level observed in the control device. The presence of significant quantities of sodium in the CdTe material demonstrates the requirement for a detailed study of its effects, as it is likely to be a common impurity in all CdTe devices.

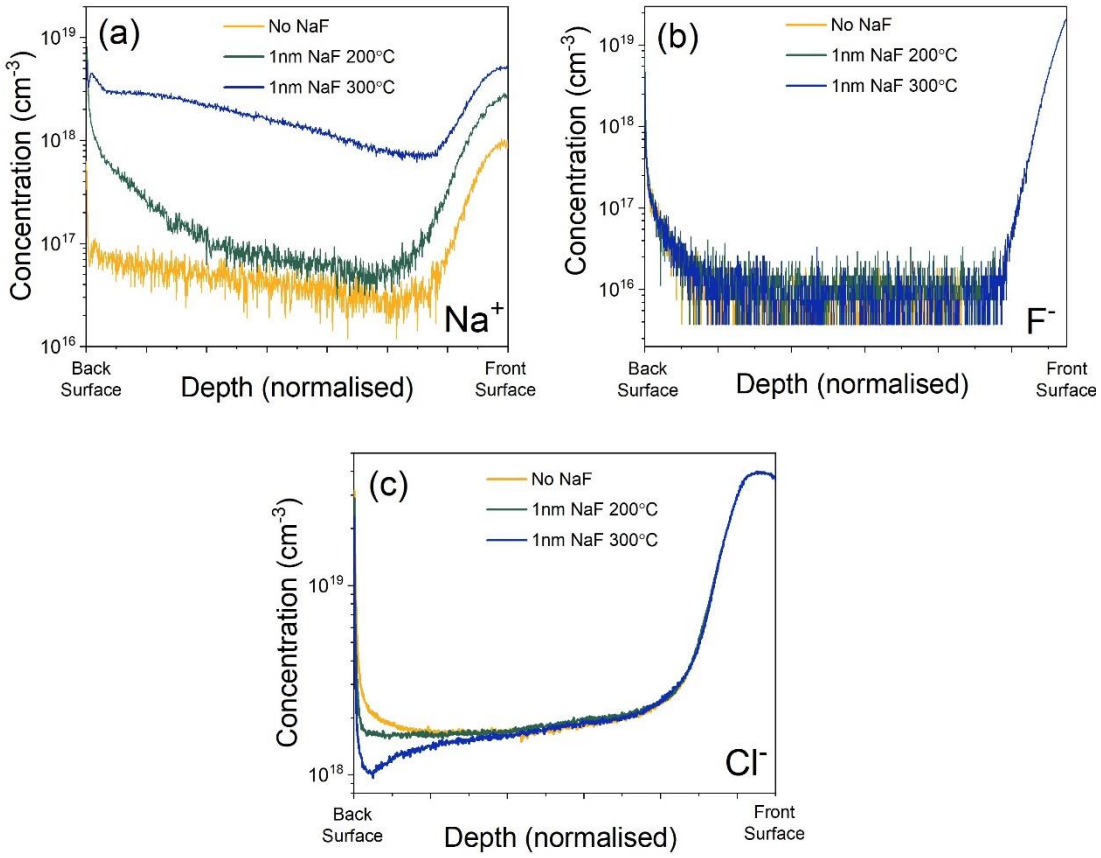

Figure 6.5: Distribution of (a) sodium, (b) fluorine and (c) chlorine obtained from ToF-SIMS measurements of devices with 1nm NaF deposited following $MgCl_2$ treatment annealed at 200°C and 300°C compared to a reference device without NaF.

Upon the addition of 1 nm NaF at the back surface and annealing at 200°C there is a large increase in the Na signal at the back surface, which gradually decreases further into the bulk following a typical in-diffusion profile [16], before increasing again at the front on the device near the CdS layer. The Te rich surface resulting from the NP etch may account for the relative ease of incorporation at the back contact, however sodium does not appear to incorporate effectively into the bulk of the CdTe with only a minor increase in comparison to the control device. Nonetheless it would appear to be mobile throughout the device, since there is

increased accumulation at the front surface. This could be accounted for if transport is dominated by rapid diffusion along grain boundaries which is expected to be far quicker than through the grain interior [17,18]. This would allow sodium to reach the CdS layer relatively easily, where its effect on device performance remains unclear. Sodium would be expected to compensate native *n*-type CdS doping by occupying a cadmium site through the formation of Na_{Cd} acceptors, which would lower the V_{bi} due to a lower net doping density. However, CdS is natively *n*-type due to sulphur vacancies and therefore it is unclear whether this Cd rich composition would lend itself to the formation of Na_{Cd} acceptors or would sit interstitially. Nonetheless it appears that sodium shows a strong preference to segregate at the junction position, consistent with previous observations by other authors [13].

For the 300°C annealed sample there is a further increase in sodium content at the front contact, however there is also a near-uniform incorporation throughout the bulk CdTe. This could indicate that the higher anneal temperature is required to drive the sodium into the grain interior, which would be consistent with the sharp change in the trend of doping density observed at this temperature in Figure 6.4. There is also a small peak in the Na profile near the back surface for the 300°C anneal, which could be due to Na incorporating more effectively in the Te rich region resulting from the NP etch.

The fluorine signal shown in Figure 6.5b shows an identical trend for all three devices regardless of the addition of NaF or the anneal temperature. Whilst fluorine would be expected to be an *n*-type dopant in CdTe when occupying Te sites, chlorine is in the same group and appears to aid *p*-type doping via the formation of complexes [19]. It is unclear whether fluorine would act in a similar manner, although it is noteworthy that there is preliminary evidence of a combined $CdCl_2$/CdF treatment showing a beneficial effect in some devices [20,21]. In any case, the absence of any additional fluorine from the NaF treatment is favourable for achieving a high doping density with a simpler defect structure, and suggests NaF is a suitable source of sodium. Diffusion of fluorine into CIGSSe solar cells during NaF treatment is inhibited by the formation of volatile SeF_6 [22]. A similar reaction to form TeF_6 might occur here and would offer a plausible explanation for the lack of excess F signal in the bulk of the CdTe layer upon NaF treatment. Despite no additional fluorine contribution in the CdTe layer from the NaF layer within the instrumental detection limits, there is a clear increase in signal towards the back surface for all devices. This could result from out-diffusion from the SnO_2:F layer at the front contact, whereby fluorine segregates out of the CdTe layer towards the back surface during device processing as seen previously by Emziane et al [23]. Impurities in the $MgCl_2$ solution and NP etch could also offer potential sources of fluorine contamination.

Figure 6.5c shows a similar chlorine content for the three devices towards the front surface and most of the bulk CdTe layer, however there is a small change at the back surface for the three devices. All samples show a very rapid increase in chlorine concentration within the first few nanometres from the back contact which is likely related to a change in sputtering yield at the surface rather than a true increase in Cl content [24]. The control device without NaF shows a large, gradual increase in Cl concentration at the back surface which is not surprising given the $MgCl_2$ activation process is likely to leave a chlorine rich region. The low temperature NaF annealed device shows a much flatter region with no gradual increase in Cl signal. Higher anneal temperature leads to a further reduction of the back-surface Cl content, leaving a slightly chlorine deficient region. It is unclear what causes this loss of chlorine and whether it has an impact on device performance, but since the chlorine deficient regions overlap with the excess sodium, some reaction involving both elements seems plausible. Considering the improvement in contacting with NaF implied in Figure 6.1, this change in chemical composition at the back surface could be beneficial for device performance.

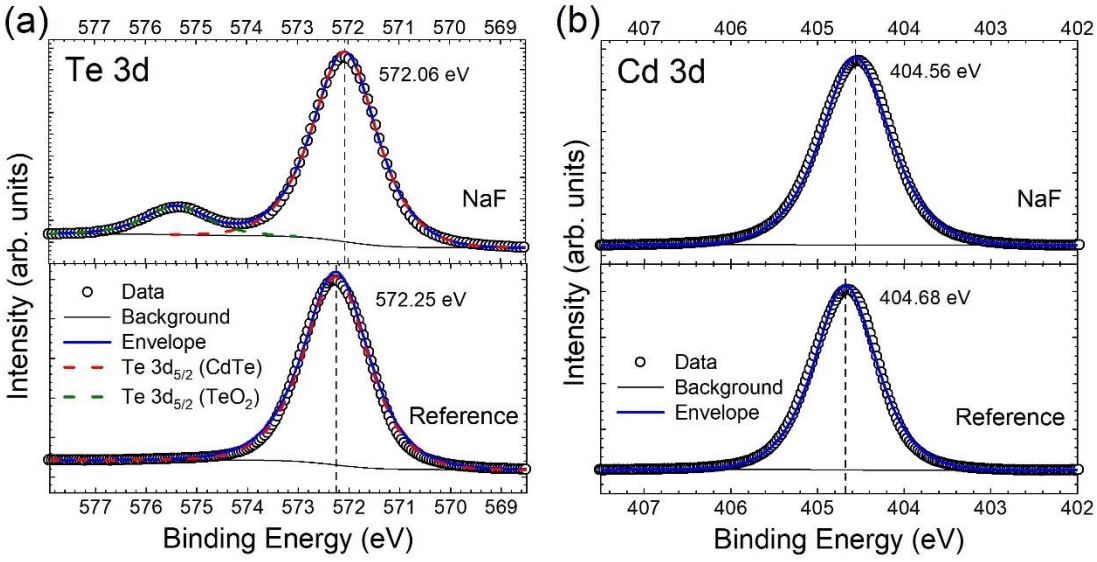

Figure 6.6: Core level XPS spectra showing the (a) Te 3d and (b) Cd 3d peaks comparing a standard CdTe device to one with 1 nm NaF evaporated at the back surface and annealed at 300°C for 20 min in air

XPS was used to determine the chemical composition of the back surface of a reference CdTe device with a simple Au contact compared to one with 1 nm NaF deposited prior to a 20 min anneal at 300°C in air. The $3d_{5/2}$ core level peaks are given in Figure 6.6 (a) for Cd and (b) for Te. The cadmium spectra in both cases can be fit with a single peak and therefore atoms are bonded only to tellurium with no contribution from sodium, fluorine, magnesium, or chlorine (within the limits of detection). While the tellurium peak for the reference device is similar, in that there is only one bonding environment, in the case of the NaF device there is a secondary peak appearing at higher binding energy corresponding to the formation of a TeO_2

oxide phase at the back surface. This oxidation is caused by the annealing step required to effectively distribute the sodium throughout the CdTe and increase the doping density, however is likely to be detrimental to device performance as it will hinder the formation of an ohmic contact [25,26]. In this case it appears the beneficial effects of doping outweigh the effects of this oxidation as this does not show the rollover observed for the reference device in Figure 6.1, however the series resistance does increase with anneal temperature which is likely caused by increasing the thickness of TeO_2. This might be overcome by annealing the devices in an inert atmosphere so that high doping densities could be obtained as well as an oxide free surface. Efforts to test this were hindered by very poor efficiencies for the entire device series, was believed to result from contaminants inside the glovebox in which anneals were performed, rather than adverse effects of annealing in an N_2 ambient.

6.2.4 Effect of 5 nm NaF treatment on CdTe solar cells

The device data shown in section 6.2.2 indicates that 1 nm NaF at the back contact is sufficient to improve the back contact quality, and annealing at 300°C leads to an increase in the net doping density. During preliminary test runs with varied NaF thickness, the addition of more than 1 nm NaF did not appear to show any benefit to device performance. There is no indication that such an NaF treatment performed after chlorine activation leads to recrystallisation of the CdTe or CdS layers observed previously [4,7,8]. However, to rule out any such effects, a series of devices were fabricated with a 5 nm NaF treatment which is expected to exaggerate any potential changes to the structure and morphology of CdTe solar cells compared to the 1 nm NaF treatment which was found to be optimal.

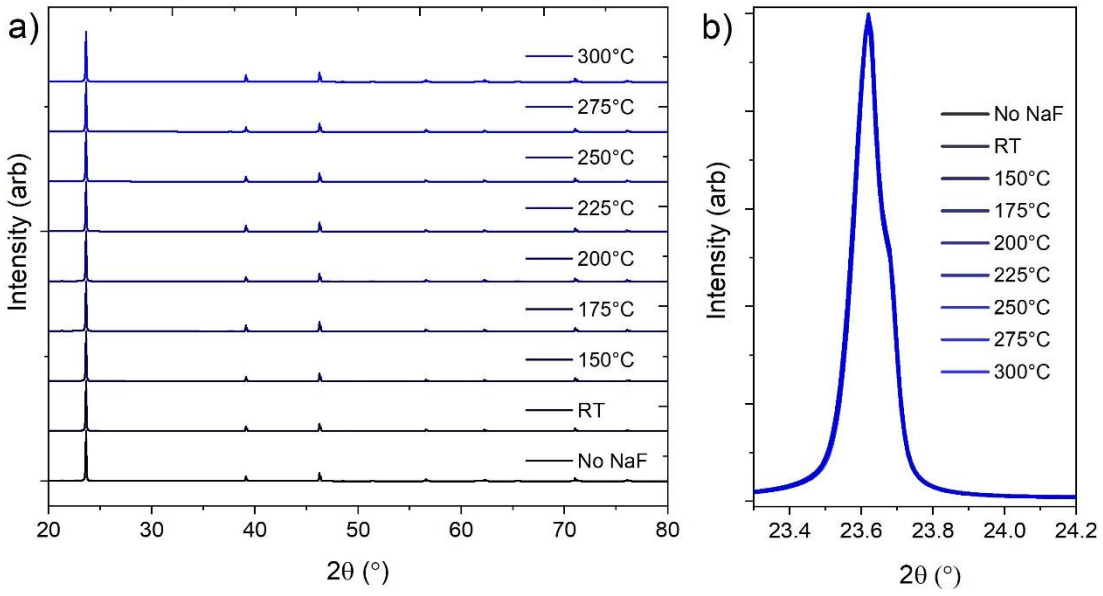

Figure 6.7: (a) stacked, normalised XRD spectra for CdTe solar cells with 5 nm NaF evaporated onto the back surface and annealed for 20 min in air between room temperature and 300°C, compared to a control device without NaF. (b) shows the same data overlaid to compare the 111 peak for each device.

Figure 6.7a shows XRD spectra collected for devices subject to a 5 nm NaF treatment and annealed at temperatures up to 300°C compared to a device without NaF treatment. In all devices, the CdTe layer remains highly 111 oriented with the dominant peak centred around 23.6 °. There is no substantial change in the intensity of the weaker reflections and therefore no evidence that the NaF treatment causes any recrystallisation of the CdTe layer. Figure 6.7b shows a closer view of the 111 peak, from which it can be seen that the peak shape is identical in all cases. Previous NaF treatments of CdTe has resulted in the intermixing of CdS and CdTe layers, resulting in the growth of a secondary peak corresponding to a CdS_xTe_{1-x} phase at slightly higher angle than the CdTe 111 peak [4]. No such effect is observed here, and instead the shoulder in the 111 peak shown in Figure 6.7b is due to reflections of K-α_2 x-rays from the Cu anode producing replica peaks at higher angle.

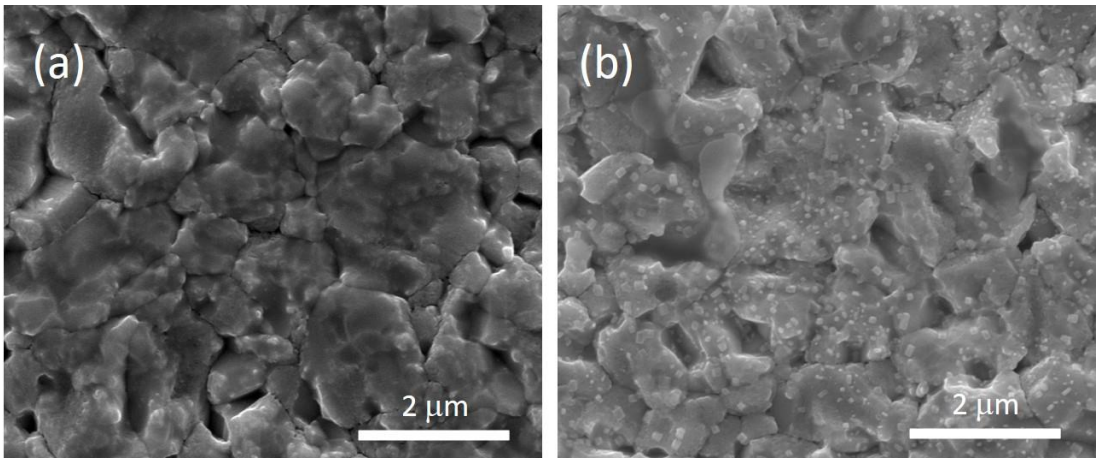

Figure 6.8: SEM image of the back surface of $MgCl_2$ treated CdTe devices after (a) NP etching, and (b) NP etching followed by deposition of 5 nm NaF and a 20 min anneal at 300°C in air

Figure 6.8 shows SEM images of $MgCl_2$ treated CdTe devices with and without a 5 nm NaF treatment. The control device without NaF treatment shown in Figure 6.8a indicates the $MgCl_2$ treatment leaves an irregular CdTe grain structure with few well-defined crystal facets. In Figure 6.8b, the NaF treated CdTe layer is similar to that of the NaF free device, but is decorated with small crystals of NaF which remain following post deposition annealing. The nominal NaF thickness of 5 nm does not form a continuous layer, but instead forms discrete crystalline islands in the early stage of film growth. There is little change in the morphology of the CdTe films in both cases, and no evidence of widened grain boundaries upon NaF treatment. This suggests that separating the NaF treatment from the chlorine activation step is indeed an effective strategy to prevent the harmful recrystallisation which has been observed for a combined Na and Cl activation treatment [7].

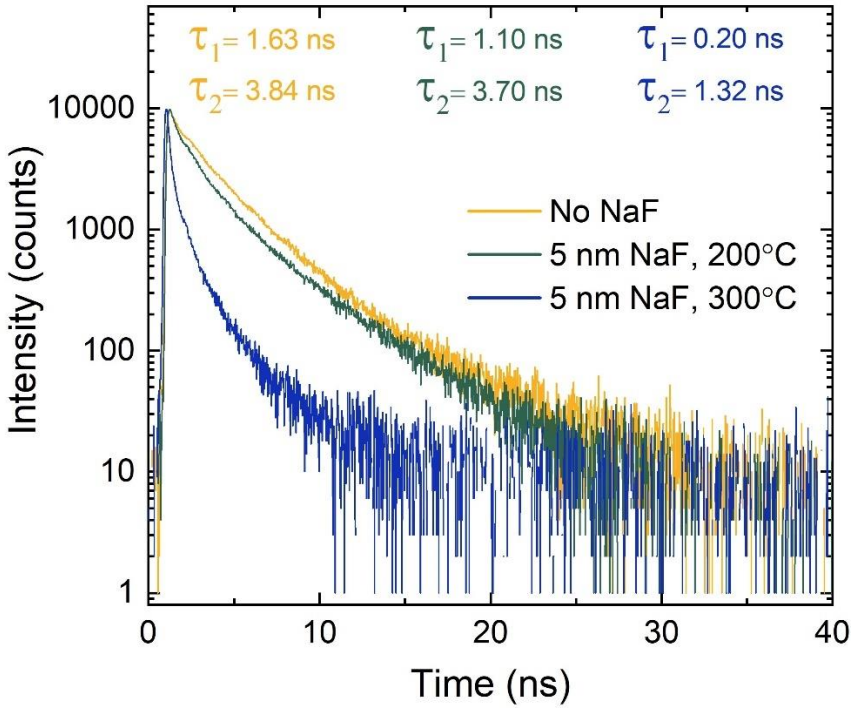

Figure 6.9: Normalised single photon excitation TRPL spectra of devices with 5nm NaF evaporated at the back surface of CdTe prior to Au contact annealed at 200°C and 300°C, compared to a control device without NaF

Figure 6.9 shows time resolved photoluminescence (TRPL) spectra measured with glass side excitation through the front surface of devices with 5 nm NaF treatment at 200°C and 300°C compared to a control device without NaF treatment. By fitting the TRPL spectra to bi-exponential decay functions (see section 4.3.6), it can be seen that there is a reduction in bulk (τ_2) lifetime in devices containing NaF to 3.70 ns and 1.32 ns for 200°C and 300°C anneals respectively, compared to the reference device with a bulk lifetime of 3.84 ns. This reduction would suggest NaF introduces new deep lying states within the band gap of CdTe despite the prediction of a shallow compensating donor [6]. Annealing NaF treated devices at 200°C results in a minor decrease in carrier lifetime compared to the control device, whereas decrease in the case of the 300°C treatment is more significant. This could be explained if the 200°C anneal results in limited sodium diffusion away from the back surface into the bulk CdTe, whereas annealing at 300°C causes bulk incorporation of sodium throughout the device. Whilst the elemental distributions shown in Figure 6.5 would agree with this interpretation, it is emphasised that these SIMS measurements are of devices with 1 nm NaF treatment compared to the 5 nm NaF used in these photoluminescence measurements. The 5 nm NaF thickness studied here is above optimal for device performance and will therefore exaggerate any changes to the CdTe absorber layer, however this reduction in lifetime suggests excess sodium incorporation is not electrically benign despite the shallow nature of both acceptor and compensating defect states [27].

Whilst this may be the case, the presence of the CdS/CdTe junction complicates the analysis. For a *p*-type material (ie. $p_0 \gg n_0$), the rate of radiative recombination of excess carriers (R_{PL}) is given by:

$$R_{PL}(t) = B \int [p_0(r)\Delta n(r,t) + \Delta p(r,t)\Delta n(r,t)]\, d^3r \qquad (6.1)$$

Where B is the radiative recombination coefficient, p_0 and n_0 are the equilibrium hole and electron concentrations, and $\Delta p(r,t)$ and $\Delta n(r,t)$ are the excess hole and electron concentrations [28]. In low injection conditions, there are few excess carriers and therefore the first term in equation (2.10) dominates, which tracks the change in excess minority carrier concentration over time and therefore should accurately reflect the minority carrier lifetime. However, the presence of a space charge region will separate electron hole pairs and sweep carriers to the edge of the depletion region. Hence the faster decay curve could also reflect enhanced charge separation due to a higher doping density and therefore increased electric field, rather than bulk recombination effects [29]. High injection conditions are therefore required, since photoinjected carriers will screen the electric field and hence more accurately determine carrier lifetime. It would therefore be necessary to compare the variation of lifetime with laser power between these samples to determine whether the presence of sodium has resulted in a decreased lifetime, which would imply deep trap levels, or the reduction in τ_2 is simply an artefact of higher doping density. If the faster TRPL decay is indeed a result of decreased carrier lifetime upon NaF treatment, it would be necessary to determine whether this is also observed for devices with a 1 nm NaF treatment which was found to be optimal for device performance.

6.2.5 Discussion

The evaporation of a thin layer of NaF prior to contacting CdTe solar cells has been shown to be an effective strategy for incorporating sodium into the device structure without the adverse structural effects observed elsewhere. However, the improvement in device performance has been modest even for optimised treatment conditions. This is likely due to several overlapping processes occurring during the evaporation of NaF and subsequent annealing of devices, such as oxidation of the back contact, sodium accumulation in the CdS layer and potential changes in carrier lifetime.

An improved contact is readily achievable regardless of specific processing steps, requiring only the presence of NaF at the back contact leading to an increased fill factor due to lower series resistance. Increasing the bulk doping density requires annealing devices to distribute

the sodium throughout the device, and from the grain boundaries into the grain interior. This occurs at temperatures above 300°C, increasing the doping density above the reference device, however this is accompanied by a smaller depletion width which affects the collection of deeply penetrating photons. This also leads to accumulation of sodium in the CdS layer where its effect remains unclear, whilst sodium incorporation into the bulk CdTe layer may reduce carrier lifetime. Higher anneal temperatures also result in the formation of an oxide back surface layer which gradually increases series resistance and lowers fill factor. Both V_{oc} and J_{sc} appear to be negatively affected by NaF and subsequent annealing, although this can be compensated for by the improved fill factor. The combined effect of all these processes could explain the significant scatter in efficiencies obtained for various annealing temperatures, leading to a minor overall improvement for devices annealed at 300°C compared to a reference device without NaF, which is notably the temperature required to activate sodium in single crystal CdTe devices enabling V_{oc} above 900 mV [30]. There is also a very significant amount of sodium already in the reference device, likely originating in the CdTe source material. This will partially mask the effect of the NaF treatment since there is likely to be some doping already occurring, and could explain why it is possible to obtain reasonable efficiencies despite adding no intentional dopants, whereas other labs produce devices with very poor efficiencies without the intentional addition of extrinsic dopants [31].

6.3 A combined NaF/$MgCl_2$ treatment for CdTe/CdS solar cells

Whilst the evaporation of NaF following $MgCl_2$ treatment is effective to some extent in doping CdTe, there has not been the drastic increase in acceptor concentration seen by Kranz et al [4], nor a significant improvement in overall device efficiency. Therefore, further attempts follow a similar approach used previously by other authors to increase acceptor concentration by depositing NaF prior to $MgCl_2$ treatment in a combined Na and Cl treatment. All previous attempts at combining the $CdCl_2$ treatment with NaF have been performed on CdTe films deposited at a low substrate temperature, which typically result in a small as deposited grain structure. Where others have experienced issues with recrystallization of CdTe grains, widening grain boundaries and excessive CdS-CdTe intermixing upon combining the Na and Cl treatment, it was anticipated that high temperature CdTe growth via CSS, which results in

large grain as deposited, may avoid this. It has previously been shown that large CdTe grains do not undergo significant recrystallisation during typical $CdCl_2$ processing, whereas small CdTe grains do [32]. Furthermore, in the case of CSS deposition the CdTe-CdS intermixing at the interface is dominated by the thermal history of the device during the CdTe growth stage rather than during the $CdCl_2$ activation [33]. A combined NaF and $MgCl_2$ treatment is therefore studied here for devices with CdTe layers grown via CSS to determine whether this device structure is more stable against sodium induced recrystallisation.

6.3.1 Device fabrication

Initial samples to compare the influence of NaF on the $MgCl_2$ treatment of small grain and large grain CdTe were deposited via sputtering and CSS respectively. In each case, CdTe films were deposited on TEC 15M substrates coated with 100 nm CdS. Sputtered CdTe films were deposited at a substrate temperature of 300°C (5 mTorr Ar, 1.32 W/cm^2) to a final thickness of 2.5 μm, which had previously been optimised for sputtered CdTe devices [34]. CdTe films grown via CSS were deposited at a substrate temperature of 510°C under 30 Torr N_2, with a thickness of ~5 μm required to ensure suitable coverage. Both sputtered and CSS films were compared in their as deposited state, following $MgCl_2$ treatment at 410°C, and after the evaporation of 5 nm NaF at the back surface prior to $MgCl_2$ treatment at 410°C.

Sputtered CdTe films were found to be unsuitable for further processing into full devices and therefore only CSS deposited CdTe devices were produced, as described in section 6.2.1. After CdTe deposition, samples were immersed for 15 s in NP etch, dried, and immediately loaded into the evaporator for NaF deposition. Between 0 – 20 nm NaF was deposited to cover a similar parameter space to that explored previously [4], followed by $MgCl_2$ treatment at 410°C in air for 20 min. Finally, a further 15 s NP etch was performed and nine Au contacts per device were deposited through a 0.25 cm^2 mask to a thickness of 50 nm.

6.3.2 Preliminary studies on NaF induced recrystallization of CdTe/CdS films

The stability of CdTe deposited by sputtering and CSS against excessive recrystallization is compared here to understand the interrelation of deposition method and a combined NaF and $MgCl_2$ treatment. The grain structure of CdTe films is strongly affected by the growth method, and more specifically by the substrate temperature during deposition [35]. An initial assessment is needed to determine if large CdTe grains resulting from high temperature growth methods might enable the increased doping density seen previously without the accompanying morphological changes that would prove detrimental to device performance [4]. CdTe films grown by sputtering (T_{sub} = 300°C) and CSS (T_{sub} = 510°C) onto CdS/TEC15M substrates

were used to compare the morphology of as deposited films with $MgCl_2$ treated films and those having undergone a combined NaF and $MgCl_2$ treatment.

Figure 6.10a shows the surface of a sputtered CdTe film as deposited with small, uniform and compact grains typical for sputter deposition. The low substrate temperature means that the critical radius required for adatoms to nucleate is easily achieved, leading to densely packed nucleation sites which template further growth of many small grains [36]. Following $MgCl_2$ treatment (Figure 6.10b), there is a small increase in grain size as the CdTe recrystallizes driven by a minimization in surface energy [32]. There are also numerous pinholes that form where the aggressive recrystallization has left areas of the underlying substrate exposed, which is commonly observed for sputtered CdTe films [34]. Clearly these films would not produce working devices, but it does demonstrate the sensitivity small grain CdTe films towards recrystallization. The evaporation of 5 nm NaF prior to $MgCl_2$ treatment results in further grain growth as show in Figure 6.10c, with more clearly defined crystal facets. Grain growth is generally beneficial for device performance since the decrease in grain boundary density will reduce recombination. However, SEM images of the same film at lower magnification, shown in Figure 6.11d, indicate that this grain growth is accompanied by large areas of exposed underlying substrate, far more severe than those observed for $MgCl_2$ treatment alone. This renders films semi-transparent to the eye and again unsuitable for further device processing, in a similar albeit more drastic presentation of effects shown in MOCVD and evaporated CdTe films [4,7].

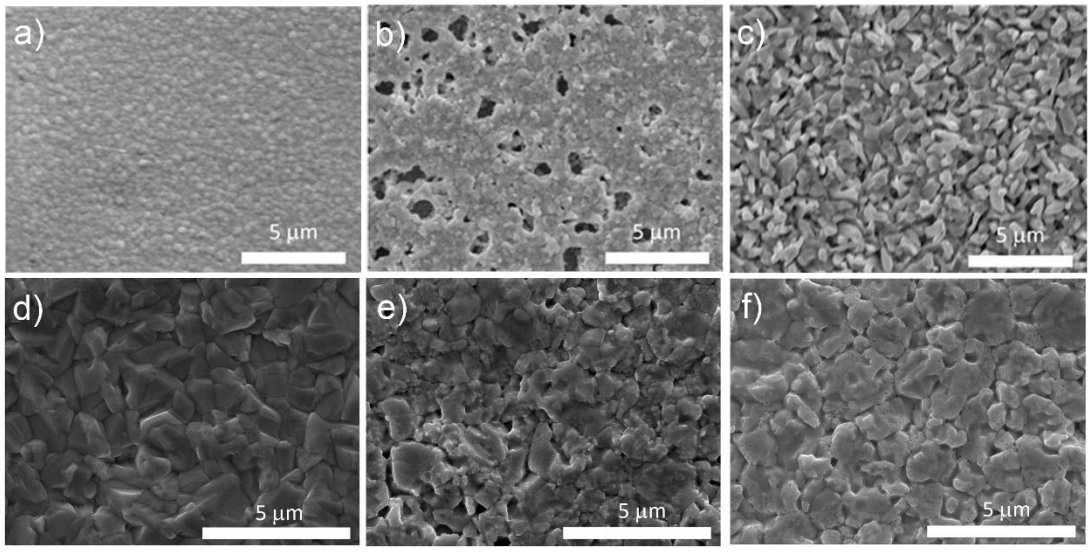

Figure 6.10: SEM images of the CdTe films grown by sputtered (top) and CSS (bottom), showing the morphology of films as grown (a, d), $MgCl_2$ treated (b, e) and $MgCl_2$ treated following deposition of 5 nm NaF (c, f)

Growth of CdTe films via CSS typically results in much larger as deposited grains, demonstrated in Figure 6.10d, due to higher substrate temperature reducing the lifetime of an adatom on the surface, reducing the probability of a stable nucleus forming. This results in relatively few nucleation sites and therefore a smaller number of large grains. The large grain films are more stable to chlorine induced recrystallisation, showing little evidence of grain growth since the already large grain size does not provide a strong driving force for recrystallization. Therefore it is reasonable to expect that CSS films are similarly stable against enhanced NaF/$MgCl_2$ recrystallization that proved detrimental to sputtered films. Although the aggressive nature of $MgCl_2$ treatment does alter the morphology of the CdTe back surface (Figure 6.10e) leading to reduced definition of grain boundaries, there is no evidence that this effect is enhanced with the addition of 5 nm NaF prior to chlorine treatment (Figure 6.10f).

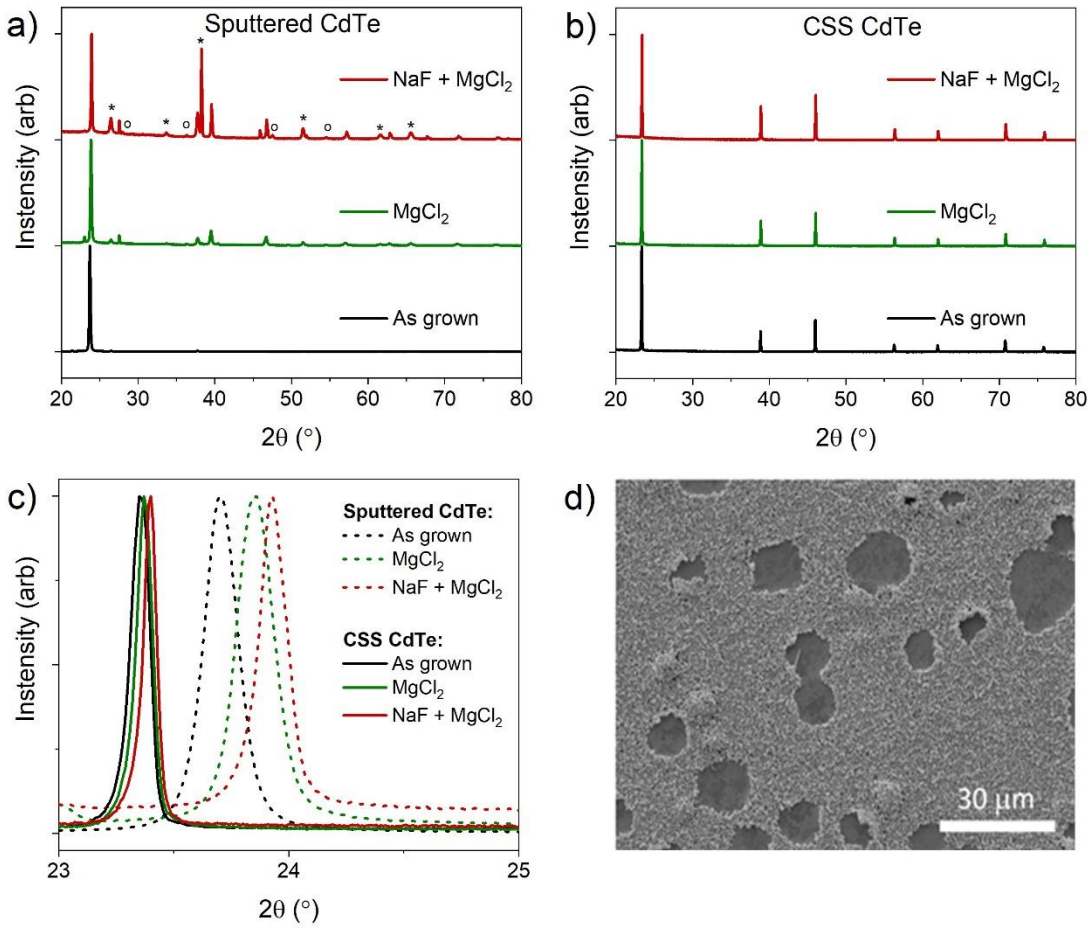

Figure 6.11: XRD spectra of CdTe grown via sputtering (a) and CSS (b) for films as deposited, $MgCl_2$ treated, and a combined NaF & $MgCl_2$ treatment, as well as a comparison of the 111 peak (c). Peaks corresponding to CdS (o) and SnO_2 (*) have been labelled. An SEM image of NaF & $MgCl_2$ treated CdTe deposited via sputtering shows large areas of exposed substrate (d).

This stability against recrystallization for CSS films is further shown in the XRD spectra in Figure 6.11. The sputtered CdTe films in Figure 6.11a are nearly exclusively (111) oriented as deposited, with the peak centred around 24°, with strong preferential orientation common for low temperature growth methods [37]. After $MgCl_2$ treatment, recrystallization of grains causes other peaks to become visible, although it retains the (111) preferential orientation. Evaporation of NaF prior to $MgCl_2$ treatment has a similar effect, but the recrystallisation is more pronounced resulting in a more randomized grain texture. There is also a significant signal from the CdS and SnO_2 layers underneath the CdTe, due to the exposed substrate areas shown in (d). This is not the case for CSS grown films in (b), which show little difference between the as-grown and treated films. Whilst there is still a clear (111) preferential orientation, the as-grown film shows a strong signal from other orientations which is not seen for as grown sputtered CdTe. The intensity of these peaks is not changed significantly with $MgCl_2$ treatment nor with the combined NaF and $MgCl_2$ treatment, indicating the CSS grown CdTe is much more stable compared to the sputtered CdTe.

This XRD data can also be used to assess the degree of intermixing between the CdTe and the underlying CdS layer, which is also reportedly enhanced by the NaF treatment [4], by looking more closely at the position of the (111) peak. This is compared in Figure 6.11c for both CSS and sputtered material. The as grown sputtered CdTe peak is centred very close to the expected position for stress-free (powdered) CdTe at 23.76°. This peak is shifted to a higher angle following $MgCl_2$ treatment, and even more so with a combined NaF and $MgCl_2$ treatment. This can be explained by considering the CdS-CdTe interdiffusion that occurs during chlorine treatment. The substitution of sulphur onto tellurium sites decreases the average lattice spacing due to its smaller atomic radius, increasing the diffraction angle. In this way, the movement of the (111) peak is used as an indicator for the extent of CdS-CdTe intermixing. Whilst sodium and/or fluorine incorporation into the lattice might be expected to yield similar results, the small amount of NaF layer used here would not be sufficient to produce the observed peak shifts. Hence we can infer that for the sputtered material CdS/CdTe significant interdiffusion is occurring during $MgCl_2$ treatment and there is further enhancement due to the addition of NaF. Sodium is expected to have the dominant effect on recrystallization and intermixing as opposed to fluorine, since a similar effect has been seen in other work with NaCl [4,5]. This is supported by observations that fluorine does not readily incorporate into CdTe films, instead segregating at the back of the device, especially upon chlorine processing [38], as well as SIMS measurements in Figure 6.5 showing no evidence of additional fluorine incorporation from NaF.

A similar trend is observed for CSS grown CdTe. The as grown peak is centred at 23.37°, which is slightly below the value expected for a CdTe powder likely due to changes in the

tensile stress for the CSS grown film increasing the average lattice spacing and therefore decreasing the diffraction angle. The shift to higher angles for the $MgCl_2$ treated, as well as NaF and $MgCl_2$ treated films, likely indicates some interdiffusion of the CdS and CdTe films is occurring during treatment. The extent of this interdiffusion appears to be significantly less pronounced than for sputtered CdTe films, indicated by the smaller changes in peak position. However, this is not conclusive evidence since there will be some influence from the thicker CSS grown CdTe film compared to sputtered CdTe meaning a reduced NaF as well as Cl content per volume of material and therefore less pronounced intermixing. X-rays also need to probe deeper into the sample to reach the CdS/CdTe interface compared to sputtered samples, hence the signal from this region is weaker.

The SEM and XRD data presented here shows the inclusion of NaF in the $MgCl_2$ treatment clearly has a significant impact on the recrystallization of sputtered films. It not only leads to grain growth but also exposes large areas of underlying substrate, preventing further device processing. This recrystallization appears to be effectively inhibited by using high temperature depositions methods such as CSS to prevent these adverse morphological changes. The mechanism by which this recrystallization is enhanced remains unclear, however relies on both Na and Cl being present (i.e. treatment NaF alone does not promote growth). It should also be noted that NaCl is not an effective means of introducing sodium and chlorine simultaneously. This may be caused by the inability of NaCl to dissociate in this temperature region and therefore is not an effective source of chlorine [39]. Since Cl acts to produce a low melting point eutectic in CdTe-$CdCl_2$ pseudobinary phase diagram [40], it is feasible that addition of Na could act to further reduce this eutectic point allowing for more efficient recrystallization, especially given the prevalence of use of an NaCl flux in wide range of material systems. An investigation of CdTe with $MgCl_2$ and NaF using DSC/TGA was abandoned due to the unexpected disassociation of Cd-Te at low temperatures, but further study in this area could pinpoint the mechanism behind grain growth, which might be used to better inform more effective chlorine processing in the future.

6.3.3 CdTe/CdS solar cells with NaF deposited prior to $MgCl_2$ treatment

Having shown that growth of CdTe by CSS allows for films to undergo a combined NaF and $MgCl_2$ treatment whilst maintaining continuous substrate coverage, full solar cells are then made with between 0 – 20 nm NaF deposited prior to chlorine treatment.

6.3.3.1 JV, EQE and CV analysis

Figure 6.12 shows that the performance of devices is strongly affected by the amount of NaF present during chlorine treatment, with thicker NaF layers leading to a deterioration in all device parameters. Whilst the efficiency decreases with progressively more NaF, the open circuit voltage decrease is most apparent between 1 – 10 nm NaF before levelling out around 0.4 V. The short circuit current density for the highest efficiency devices does not decrease until more than 10 nm NaF is applied after which it begins to decrease rapidly. The fill factor gradually decreases for all NaF thicknesses as a result of both increased series resistance and a rapid lowering of shunt resistance. Several cells from devices with >10 nm NaF showed no rectifying behaviour. Despite the previous observations that CSS devices are more stable against CdTe recrystallization, the addition on NaF is clearly deteriorating the diode response of the CdS/CdTe junction meaning carriers are not efficiently separated and the solar cell is merely acting as a conductor. A similarly rapid drop in shunt resistance with the addition of NaF was observed by Kranz et al [4], and is attributed to widened grain boundaries in the CdTe layer providing shunting pathways, and excessive intermixing at the CdS/CdTe junction. Since no widening of grain boundaries was observed in this study, this can be ruled out as the dominant reason for reduced shunt resistance.

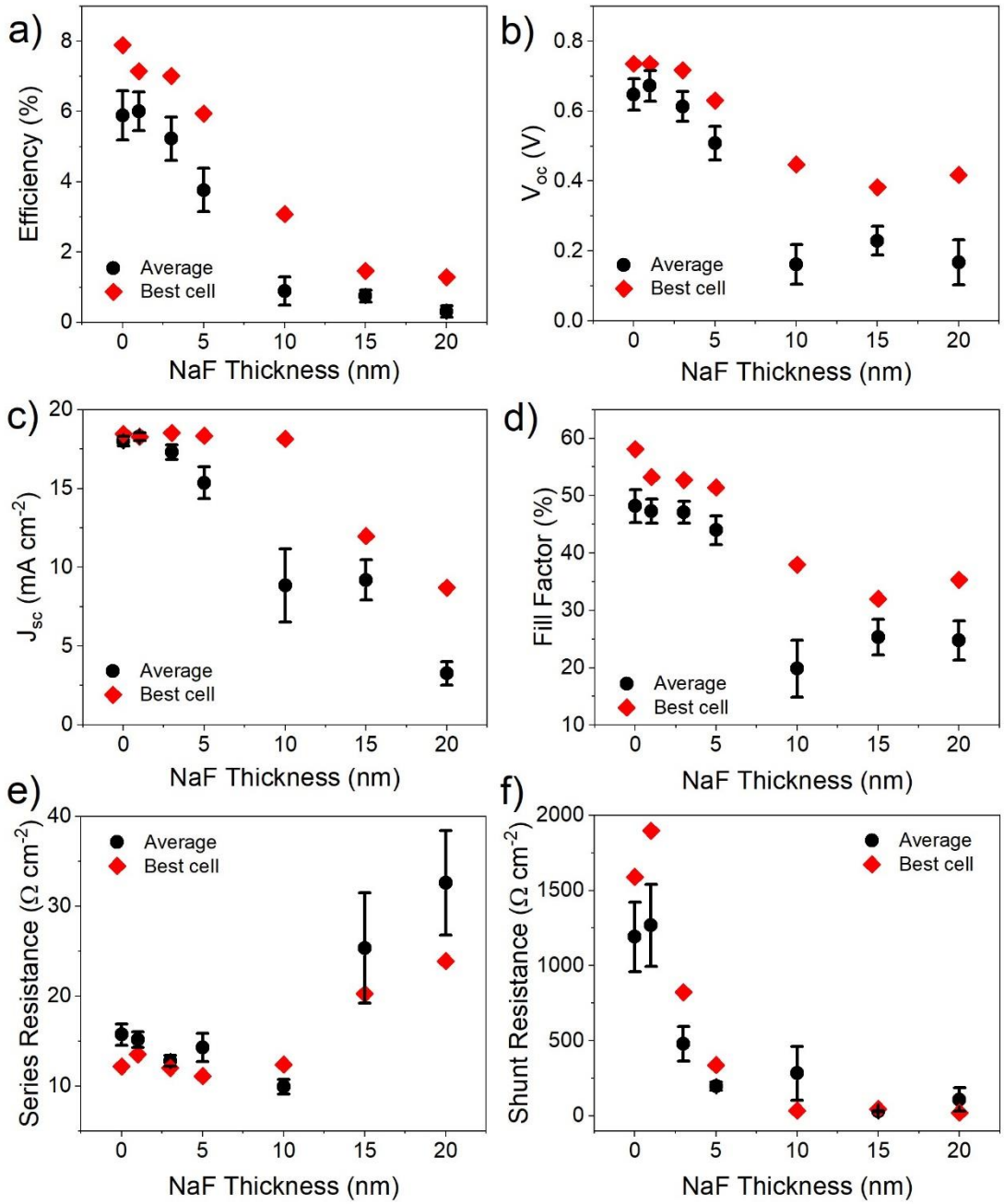

Figure 6.12: *JV* parameters for CdTe/CdS devices with 0-20nm NaF deposited at the back surface prior to $MgCl_2$ treatment at 410°C for 20 min. The peak and average efficiency (a), open circuit voltage (b), short circuit current density (c), fill factor (d), series resistance (e) and shunt resistance (f) is given as a function of NaF thickness.

Figure 6.13 shows the *JV* curves from the highest efficiency contact of the devices described above. The addition of up to 5 nm NaF does not significantly affect the shape of the *JV* curves near short circuit conditions. These devices showing a reasonable diode shape with distinct turn-on voltage, although V_{oc} and fill factor is reduced as NaF thickness is increased. Devices with more than 5 nm NaF show a much poorer diode response, with current density varying significantly with applied voltage near J_{sc}. This voltage dependent current collection near short circuit indicates charge carriers are not effectively separated by the internal electric field of

the solar cell and therefore photocurrent continuously decreases as the field is lowered in forward bias [41]. Since there is no widening of grain boundaries observed upon NaF incorporation, it is unlikely that charge transport via shunting pathways, bypassing the p-n junction, is responsible for the reduced shunt resistance. Instead, the junction quality itself deteriorates upon NaF addition resulting in a poor diode response.

Although the control device without any NaF results in the highest efficiency, it also shows the most severe rollover in forward bias. This current limiting effect is reduced for the 1 nm and 3 nm devices and is not observed at all for NaF thicknesses above this. It was demonstrated in section 6.2.2 that a NaF treatment following $MgCl_2$ activation eliminates rollover, presumably due to the formation of p^+ region resulting in a lower barrier height. Whilst it is possible that a similar effect is observed here, temperature dependent *JV* measurements would be required to provide more compelling evidence of an improved back contact. In any case, the deterioration of the shunt resistance and poor diode response far outweighs any potential benefit of improved contacting with a combined NaF/$MgCl_2$ treatment on these devices.

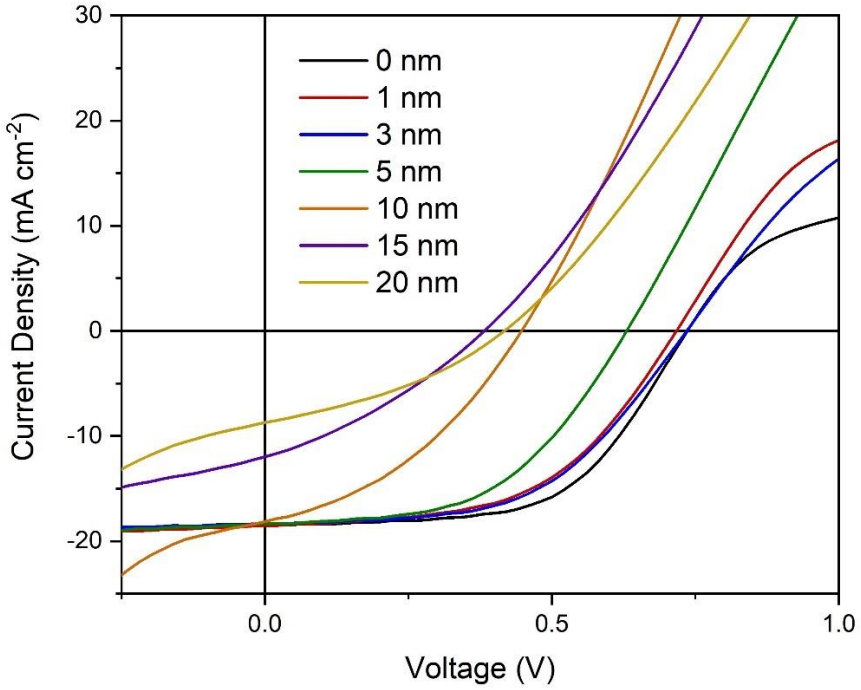

Figure 6.13: *JV* curves from measurements of the highest efficiency cell of devices with 0 – 20 nm NaF evaporated onto the CdTe back surface prior to $MgCl_2$ activation at 410°C for 20 min in air

Figure 6.14 shows the external quantum efficiency of the best performing cells, and the same curves normalised to the point of highest EQE response to allow easier comparison. This can explain the decreased shunt resistance observed upon NaF incorporation, since the clearest change in the normalised EQE is the increased collection below 500 nm for devices with thick NaF layers which is typically associated with a reduction in the thickness of the CdS layer. Although the CdS layer does contribute to parasitic absorption of high energy photons, the

consumption of this layer means a poor-quality junction may be formed with the underlying SnO_2 which is not as effective in separating charges. This lowers absolute collection efficiency across all wavelengths as shown in Figure 6.14a.

There are two potential causes for the reduced CdS absorption observed either a) excessive intermixing of CdS and CdTe results in consumption of the CdS layer, or b) significant recrystallisation of the CdS has occurred leading to higher transparency of the CdS due to voiding. Some change in the degree of intermixing is probable given the shift of the (111) peak with the addition of NaF shown in Figure 6.11, however some characteristics associated with increased intermixing are lacking from the EQE curves. Te interdiffusion into the CdS forms a lower bandgap $CdS_{1-x}Te_x$ region which reduces EQE response in the ~520-550nm range [42]. Additionally, diffusion of sulphur into the CdTe layer can reduce the bandgap via the band bowing effect, increasing the EQE cutoff to longer wavelengths in a similar manner to that exploited via Se incorporation [43]. Neither of these features are strongly apparent in the EQE data. It therefore seems likely that while some additional interdiffusion is possible, the lack of key indicators of this in the EQE spectra means that the decrease in CdS parasitic response is more likely due to recrystallisation of the CdS as observed by both Krantz et al [4] and Durose et al [5].

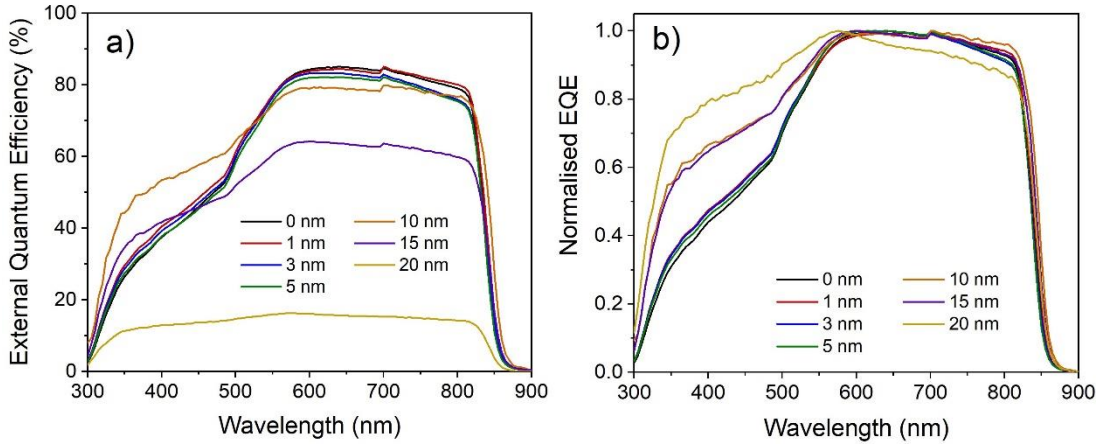

Figure 6.14: EQE of highest efficiency contacts from CdTe/CdS devices with 0-20nm NaF deposited prior to $MgCl_2$ treatment (a), as well as the normalised curves (b)

Previous studies have shown that the interdiffusion between CdS and CdTe for a typical CSS device is dominated by its thermal history whereby higher substrate temperatures during growth encourage more interdiffusion, with no evidence of further mixing during chlorine treatment [33]. This is not the case for low temperature growth methods where the chlorine treatment strongly affects the sulphur distribution [44]. Irrespective of whether the increase in the blue response of EQE measurements shown in Figure 6.14 is due to recrystallisation of the CdS layer itself, interdiffusion with the CdTe layer or some combination of the two, this is not typical for CdTe devices grown via CSS. Whereas high temperature growth normally

determines the eventual sulphur profile within a CdTe device [33], the addition of NaF to the chlorine treatment is clearly resulting in significant redistribution of the CdS layer, to the detriment of device performance.

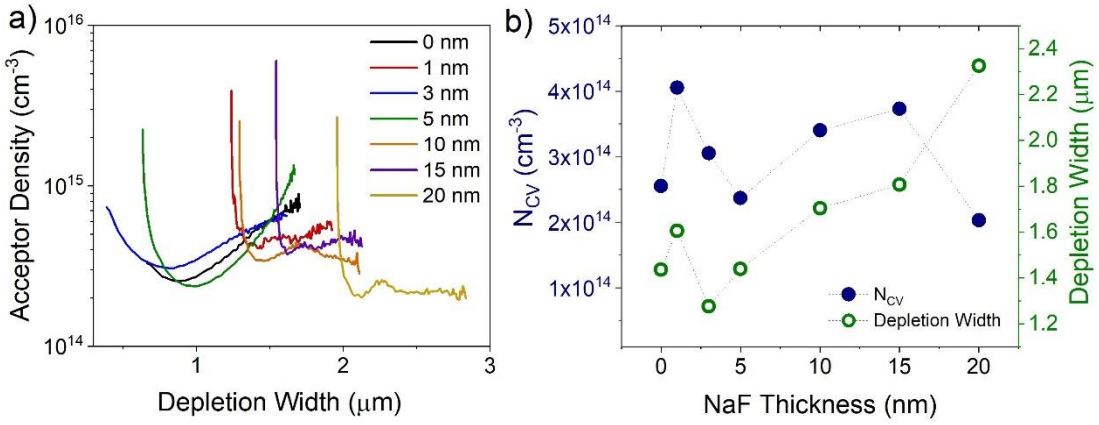

Figure 6.15: Acceptor density vs depletion width plots from *CV* measurements of CdTe/CdS devices with 0-20nm NaF deposited at the back surface prior to $MgCl_2$ treatment (a), with the doping density taken from the minima of these curves and depletion width at 0 V bias shown in (b)

Figure 6.15 shows results from *CV* analysis of the devices with 0 – 20 nm NaF deposited at the back surface prior to chlorine activation, which is used to determine bulk doping density from the minimum of the acceptor density profiles. Although at first glance the curves shown in Figure 6.15a may indicate a shift in the depletion region away from the CdS/CdTe interface for increasing NaF thickness, there is no indication of a buried junction in EQE data. Considering the complexities encountered in *CV* measurements of CdTe solar cells, this interpretation may be too simplistic and does not account for other affects such as a rectifying back contact which can artificially increase the acceptor density at either side of the U-shaped profile [45], and could potentially explain the apparent shift in junction position. Given that the addition of NaF leads to the deterioration and possible consumption of the CdS layer, it is not clear which junction is being probed by the *CV* measurements, and is likely a combination of CdTe/CdS, CdTe/SnO_2 and CdTe/Au junctions, making interpretation of this data difficult. However, it is clear that for all devices tested the bulk doping density remains around 10^{14} cm^{-3}, with no obvious trend as a function of NaF thickness. This contrasts with Kranz et al. [4] who found an increased acceptor density in evaporated CdTe/CdS devices with increasing NaF thickness. The lack of change in the doping density, despite significant impact upon device structure due to the presence of Na, indicates strong compensation of any Na-induced acceptors by Na interstitials. Alternatively, it may indicate that a higher annealing temperature is required to effectively incorporate the Na as a dopant. Given the deleterious impact of the current temperature used for this device structure, any such increase would further compromise performance. Furthermore, results presented in section 6.2.3 indicate that Na can be incorporated into CdTe at temperatures below 400°C.

6.3.3.2 Structural characterisation of NaF treated CdTe/CdS solar cells

Figure 6.16 shows XRD data for the devices discussed above. For NaF thicknesses above 5 nm, all CdTe peaks are asymmetrically broadened resulting in a shoulder towards higher angles. This is observed most clearly for the (111) peak shown in Figure 6.16b. This asymmetric peak broadening is due to the emergence of a secondary peak at a slightly higher angle compared to the CdTe peak, corresponding to a sulphur rich CdS_xTe_{1-x} phase [444]. The appearance of a distinct second peak instead of a steady shift of peak position indicates two distinct phases of CdS_xTe_{1-x} and CdTe, rather than gradual variation of the sulphur content due to the miscibility gap in the CdS-CdTe system. No peaks from the hexagonal CdS substrate are observed, which may be entirely converted into the CdS_xTe_{1-x} phase evidenced by the lack of absorption in EQE data, or not detected in these measurements due to the limited penetration depth of the x-rays in CdTe.

The texture coefficient for the 7 CdTe peaks visible in the range 20-80° is given in Figure 6.16c, and indicates that there is no recrystallization of the bulk CdTe layer, in contrast to observation in sputtered CdTe films. Amirkhalili [7] notes randomisation of the CdTe texture via an increase of the (400) and (220) peak intensity with the addition of NaF to the $CdCl_2$ treatment, however no such randomisation is observed here in a consistent way, with neither the 400/220 peak intensities nor the standard deviation shown in (d) following a clear trend with NaF thickness. This difference may be attributed to MOCVD growth of CdTe resulting in strong recrystallisation with $CdCl_2$, which is enhanced with NaF but not observed for higher temperature and therefore larger grained CSS growth.

The emergence of several small peaks corresponding to the Te is apparent for increasing NaF thickness is indicated in Figure 6.16a. These peaks are seen more clearly in Figure 6.17, which shows the diffraction pattern in the region close to these emerging peaks more clearly, along with the expected position of Te peaks. The presence of these metallic Te regions, which increases with NaF thickness, further explains the poor efficiency and low shunt resistance of devices with combined NaF and $MgCl_2$ treatment since they will provide highly conductive paths which act to short circuit the cell.

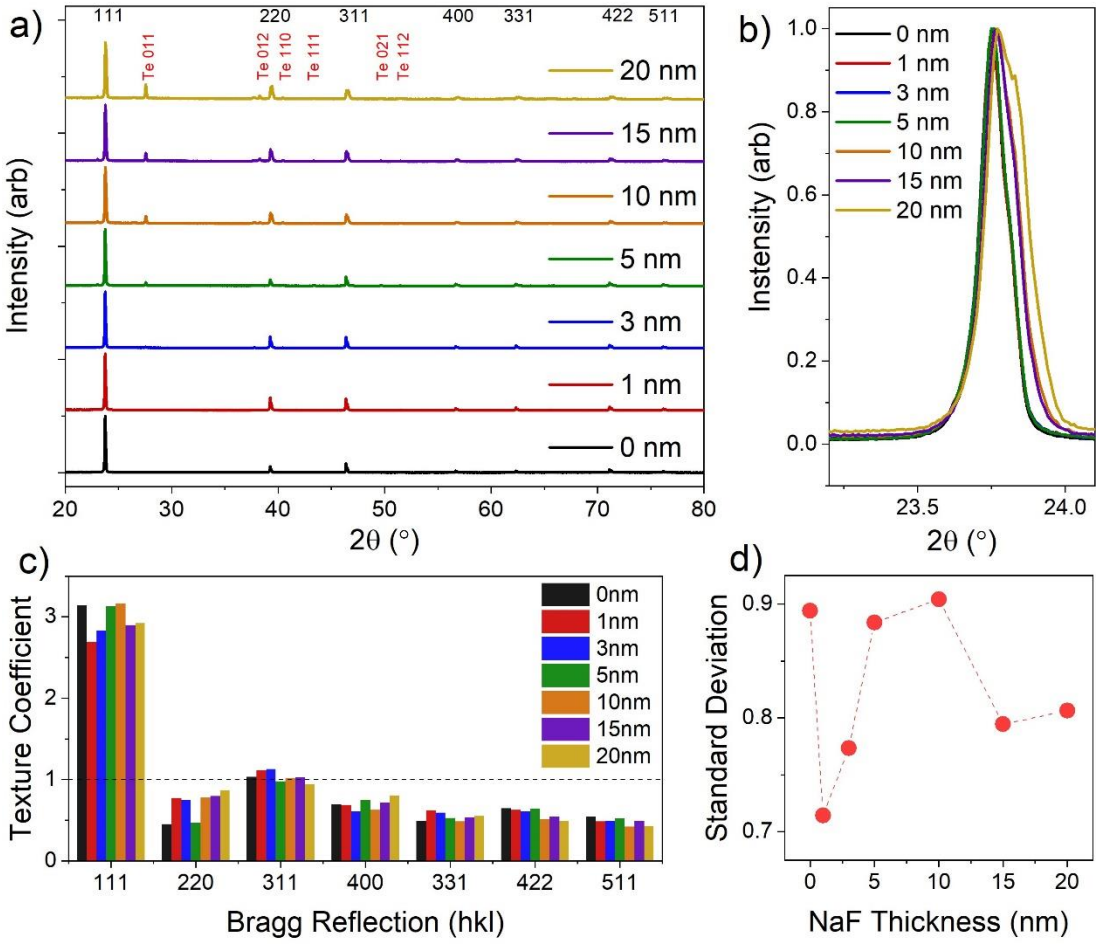

Figure 6.16: XRD data for CdTe/CdS devices with 0-20nm NaF deposited prior to $MgCl_2$ treatment. (a) shows the entire spectrum collected, with the 111 peaks shown more clearly in (b). The texture coefficient for the seven CdTe reflections are given (c), as well as the standard deviation (d).

There is no evidence of these Te peaks in data presented by Amirkalili [7] or Kranz [4]. These tellurium regions are only observed when the NaF/$MgCl_2$ treatment is applied to CdTe grown on CdS substrates (see section 6.4) therefore sulphur appears to play a key role, however exactly what reaction is taking place remains unclear. The reaction of NaF and CdS to form CdF and NaS is highly energetically favourable [46], and therefore is likely to be taking place, but does not explain the excess Te. However, it is possible some of these reaction products are acting as a catalyst for further reactions which encourage Te to precipitate from the bulk. Tellurium in CdTe is known to be undergo retrograde solubility [47], and these films are intentionally grown tellurium rich to enhance *p*-type conductivity. One interpretation could be that if the presence of sodium in the CdTe-$CdCl_2$ system lowers the eutectic temperature, the temperature limit of solubility of Te in CdTe could similarly be lowered, resulting in precipitation. Alternatively, the presence of NaF could make the chlorine treated CdTe more susceptible to Cd loss during the NP etch, which already leaves regions of elemental Te, albeit in small quantities [48]. Significant further work would be required to establish the veracity of such a mechanism.

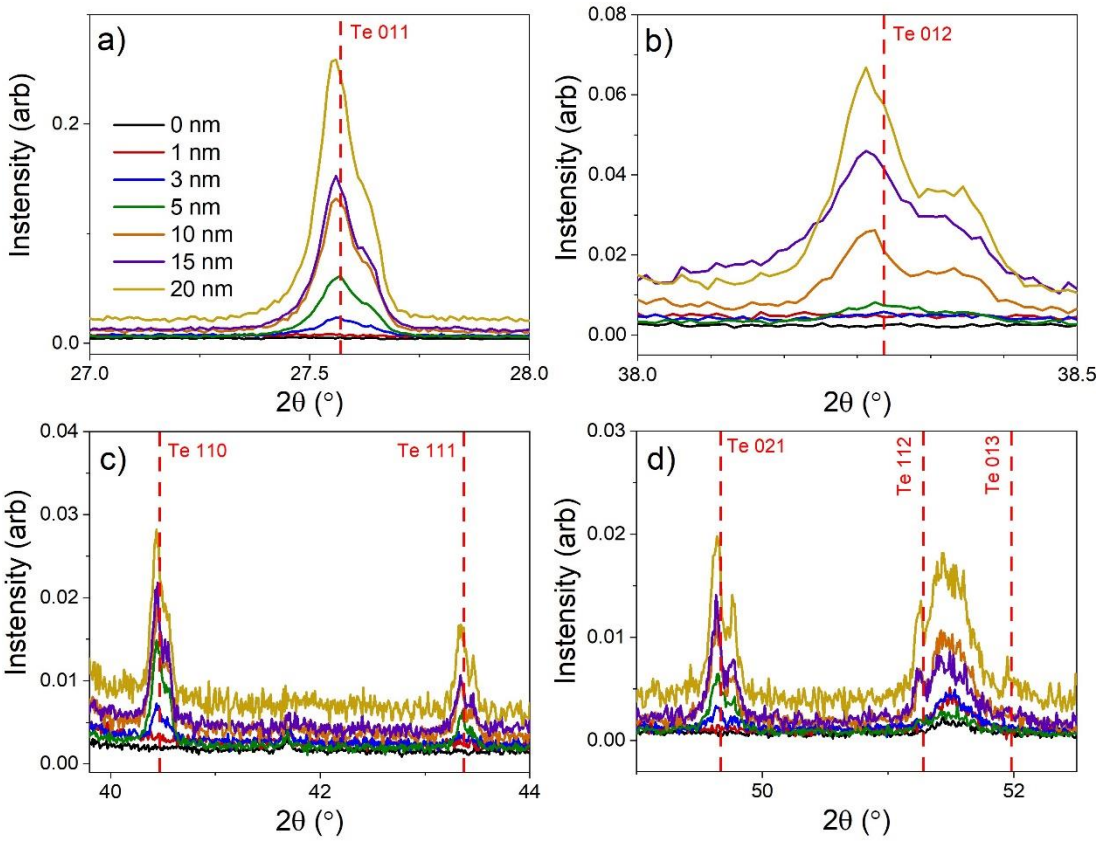

Figure 6.17: Diffraction patterns from XRD measurements of CdTe solar cells with 0 – 20 nm NaF deposited prior to $MgCl_2$ activation. Regions surrounding the expected position of Te 011 (a), 012 (b), 110, 111 (c) and 021, 112, 013 (d) peaks are shown

Figure 6.18 shows SEM images of the back surfaces of these devices with 0 – 20 nm NaF incorporated into the chlorine treatment. Neither recrystallisation of the CdTe layer or widened grain boundaries are observed for any of these films, in contrast to previous reports [7], which confirms that the CSS grown CdTe is more suitable for a combined NaF and $MgCl_2$ treatment compared to those grown at lower temperatures. For the sample with 20 nm NaF (Figure 6.18g) there is a visible semi-insulating layer which covers the CdTe and causes charging leading to poor image quality. This is likely an oxide formed during the heat treatment that is not removed effectively with the second NP etch. The presence of this oxide could account for the observed increase in series resistance shown in Figure 6.12. Further study on the effectiveness of different etchants and/or processing conditions to remove or inhibit the formation of this oxide layer would enable a better contact and therefore could offer a route to improved device performance. However, the recrystallization of the CdS layer and Te precipitates are of much greater concern for the existing device structure.

EDX analysis of the back surface allows for the elemental composition of the films to be studied. The relative cadmium and tellurium concentrations, taken from EDX measurements, are shown in Figure 6.18h as a function of NaF thickness. Below 15 nm, films appear to be

roughly stoichiometric with no discernible trend with increasing NaF thickness. It is noted that the 5 nm sample has a lower than expected Cd and Te atomic concentration due to the detection of oxygen in this film. The Cd/Te ratio decreases significantly for the 15 nm and 20 nm NaF devices, implying an increase in the relative tellurium concentration which is qualitatively consistent with XRD data shown in Figure 6.17.

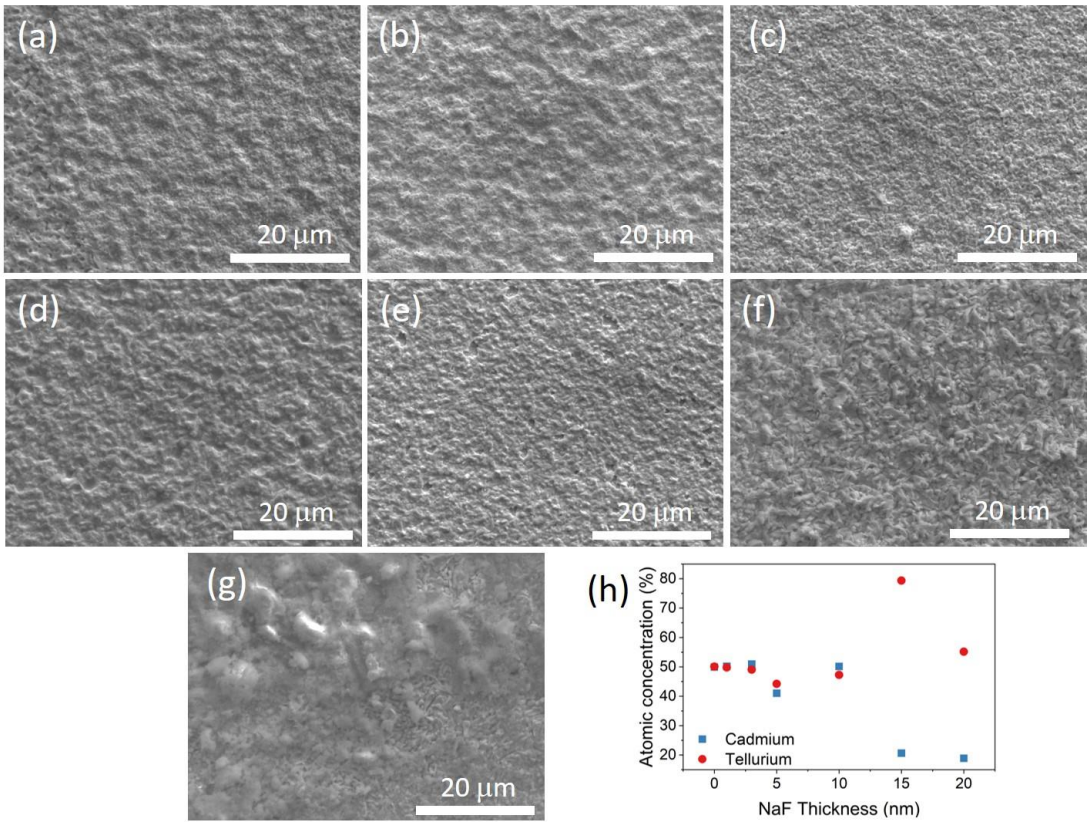

Figure 6.18: SEM images of the back surface of CdTe devices with (a) 0 nm, (b) 1 nm, (c) 3 nm, (d) 5 nm, (e) 10 nm, (f) 15 nm and (g) 20 nm NaF evaporated onto the back surface prior to $MgCl_2$ activation. The concentration of cadmium and tellurium in the absorber layer is given in (h) as a function of NaF thickness, taken from EDX measurements of the back surface.

Figure 6.19 shows cross section SEM images of CdTe/CdS devices with and without 10 nm NaF incorporated into the chlorine treatment. Figure 6.19a shows a typical device with a standard $MgCl_2$ treatment (i.e. without NaF). The CdS layer is just about visible as darker region between TCO and CdTe layers. There are several voids close to interface region due to the intermixing of CdS and CdTe layers as per the Kirkendall effect [49] which will have a detrimental effect on the junction quality. There is also a high density of stacking faults observed within most grains, which are visible as parallel lines through the grain interior. Chlorine treatment of CdTe is known to reduce the density of these stacking faults, which result in fluctuations in grain boundary potential and therefore act as hole traps [50,51]. However, clearly some remain as shown in Figure 6.19a and therefore will limit performance.

Figure 6.19b shows the cross section of a device treated with 10 nm NaF in addition to the standard $MgCl_2$ treatment. The CdTe layer in this device is much thinner than that shown in Figure 6.19a, however this is expected to result from non-uniformity during the deposition process rather than the effect of NaF. The CdS layer in this NaF and MgCl2 treated device, if present, cannot be easily distinguished from the TCO layer. Instead, there are darker regions close to the interface which are likely accumulations of CdS or CdS_xTe_{1-x} into distinct islands instead of a complete film as observed by Kranz et al [4], although EDX measurements are required to confirm this. This lack of complete window layer is consistent with EQE measurements which show increased transparency of the CdS layer upon NaF incorporation. Therefore, despite the stability of CSS grown CdTe against excessive NaF induced recrystallisation, the CdS layer remains vulnerable. This device is also largely free of the voids at the interface which were present in the NaF free device. This could be a result of the CdS recrystalising into islands rather than diffusing into the CdTe layer, thereby preventing the accumulation of vacancies which causes the voids.

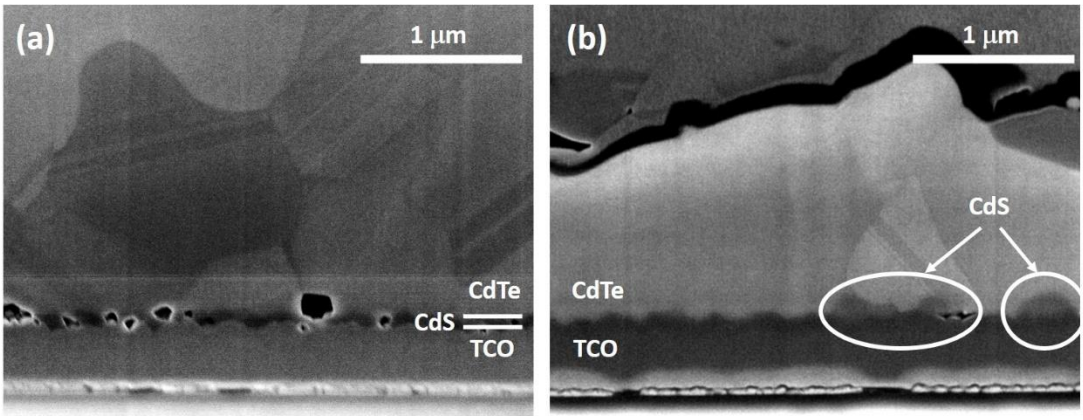

Figure 6.19: SEM images of the cross section of CdTe/CdS devices with (a) 0 nm and (b) 10 nm NaF deposited at the back surface prior to $MgCl_2$ treatment

The CdTe layer in Figure 6.19b also appears to have fewer twin boundaries, which could support the theory that the incorporation of Na into the Cl treatment further reduces the eutectic point [40] therefore encouraging the removal of these low energy defects during the activation treatment, whilst grain growth in CSS grown films is not energetically favourable due to the large grain size. However, further investigation is required to determine whether there is indeed a statistically significant difference in the twin boundary density between devices with and without NaF present during chlorine activation.

It is also noteworthy that the alkali diffusion barrier between the TCO layer and the soda-lime glass substrate does not form a continuous film in either of the images shown in Figure 6.19. The presence of large gaps in this layer, which is intended to prevent out-diffusion of species from the substrate into the active layers of the device above it, suggests that impurities such

as sodium are likely to migrate from the glass into the CdTe layer. It is not clear whether these gaps in the barrier layer are present after manufacturing or are a result of the high processing temperatures encountered during the fabrication of the solar cell. However, this highlights the importance of understanding the optoelectronic effects of impurities such as Na in CdTe as well as other PV technologies.

6.4 A combined NaF/$MgCl_2$ treatment for CdTe/SnO_2 solar cells

Recrystallization of the CdS layer as well as Te precipitation during the combined NaF and $MgCl_2$ treatment of CdS/CdTe solar cells was found to be detrimental to device performance and achieved no increase in net doping density. The primary limit with this device structure was the interaction of Na with the CdS layer which recrystalises during the heat treatment [4], leading to a lack of an effective heterojunction. In light of the recent increases in efficiency using wider band gap partner layers such as $Mg_xZn_{1-x}O$ [52] and SnO_2 [53], such oxide windows layer may offer a more robust, stable substrate on which to perform the NaF/$MgCl_2$ treatment of CdTe whilst also enabling an increase in current density. SnO_2 was used in this work as the window layer since it is commercially available and therefore offers a convenient and consistent substrate on which to test NaF/$MgCl_2$ treatments.

6.4.1 Device fabrication

A series of SnO_2/CdTe devices were fabricated by following the same CSS conditions as for CdS/CdTe solar cells as detailed in section 6.3.1, omitting the CdS sputtering step. The TEC15M substrates consist of a ~500nm SnO_2:F layer which serves as the highly conductive front contact, as well as a 100 nm undoped SnO_2 layer which forms the heterojunction with CdTe. Whilst the SnO_2/CdTe device structure with minimal optimisation is expected to result in relatively poor efficiencies, this is accepted in exchange for a reliable test structure on which to examine the effect of NaF treatment. Following a 15s NP etch, samples had between 0-20 nm NaF evaporated prior to $MgCl_2$ treatment. A further 15s NP etch was followed by contacting with 50 nm Au.

During preliminary tests, the $MgCl_2$ treatment was carried out at 410°C to remain consistent with the treatment of CdTe/CdS devices. However, the use of the SnO_2 window layer was found to require activation at a higher temperature and therefore further $MgCl_2$ treatments were performed at 430°C. Whilst similar conclusions were drawn from both device sets,

results presented here focus on the higher temperature device series which are higher efficiency and offer easier interpretation as a result of the improved diode response.

6.4.2 *JV*, EQE and *CV* analysis

Figure 6.20 shows *JV* performance data as a function of NaF thickness for CdTe/SnO_2 devices subject to a combined NaF and $MgCl_2$ treatment. Whereas the addition of any amount of NaF to the $MgCl_2$ treatment of CdTe/CdS devices has been shown to be severely detrimental for device performance, for CdTe/SnO_2 structures shown in Figure 6.20 there is a clear beneficial effect. This is a strong indication that the adverse structural changes shown previously are related to CdS instead of the CdTe layer, and that the use of a more stable window layer such as SnO_2 (which is expected to be less prone to recrystallisation and interdiffusion with CdTe) may overcome this. A similar effect may be seen with other suitably partner layers, for example MZO which could potentially offer increased V_{oc} and efficiency [54], however such device structures require careful process optimisation [55].

Both the average and champion efficiency of devices is seen to increase with the inclusion of up to 10 nm NaF, although the 3 nm device appears to deviate from the trend of the surrounding datapoints due to a poor fill factor. The addition of more than 10 nm NaF causes a sharp decline in performance due to a higher series resistance, which may be a result of the formation of oxides at the back surface not removed effectively with the standard NP etch. The peak V_{oc} of the reference device is 0.63 V, which is lower than typical for a CdS/CdTe device due to an inferior junction quality [43]. This increases gradually before reaching at a maximum of 0.74 V for 10 nm NaF, an increase of 17% compared to the control device. All devices with NaF result in a minimum of a 30 mV improvement in V_{oc}. The J_{sc} of NaF containing devices is also marginally improved compared to the reference NaF-free device until the increase in series resistance for 15 nm and 20 nm NaF causes a sharp decrease in current density. The fill factor is highly sensitive to NaF thickness, with 1 nm resulting in a ~5% increase due to a 3 Ωcm^{-2} reduction in series resistance. As the NaF thickness increases, especially beyond 10 nm, there is a drop in fill factor owing to a gradually increasing series resistance. This is presumably due to the visibly oxidised back surface, which has a slight brown tint and more $MgCl_2$ residue for thicker NaF layers. There is no clear trend in shunt resistance, although the high series resistance is accompanied by poor diode response and low shunt resistance.

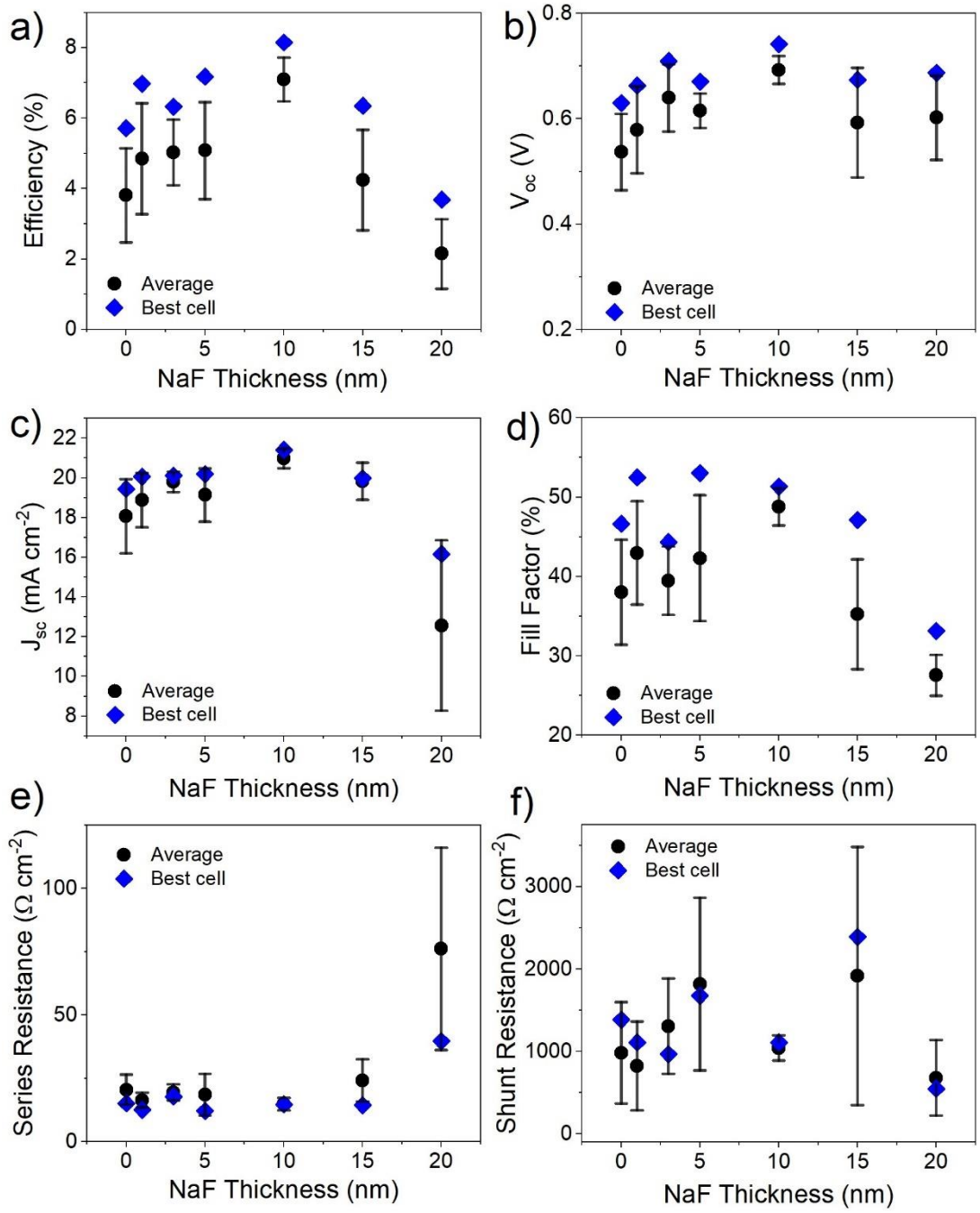

Figure 6.20: *JV* parameters for CdTe/SnO_2 devices with 0 – 20nm NaF deposited at the back surface prior to $MgCl_2$ treatment at 430°C for 20 min. The peak and average efficiency (a), open circuit voltage (b), short circuit current density (c), fill factor (d), series resistance (e) and shunt resistance (f) is given as a function of NaF thickness.

Figure 6.21 shows the *JV* curves corresponding to the highest efficiency contact from the devices described above. There is a marked improvement in V_{oc} and J_{sc} for all devices treated with both NaF and $MgCl_2$ compared to $MgCl_2$ alone, with the noticeable exception of the 20 nm NaF device. A 10 nm NaF treatment is optimal for these devices, with the further increases in thickness leading to overtreatment which reduces efficiency. The device with 20 nm appears to the heavily overtreated, showing a poor diode response and low fill factor, although the V_{oc}

remains above that of the control device without NaF. All curves show a similar degree of rollover suggesting the NaF treatment does not strongly affect barrier height.

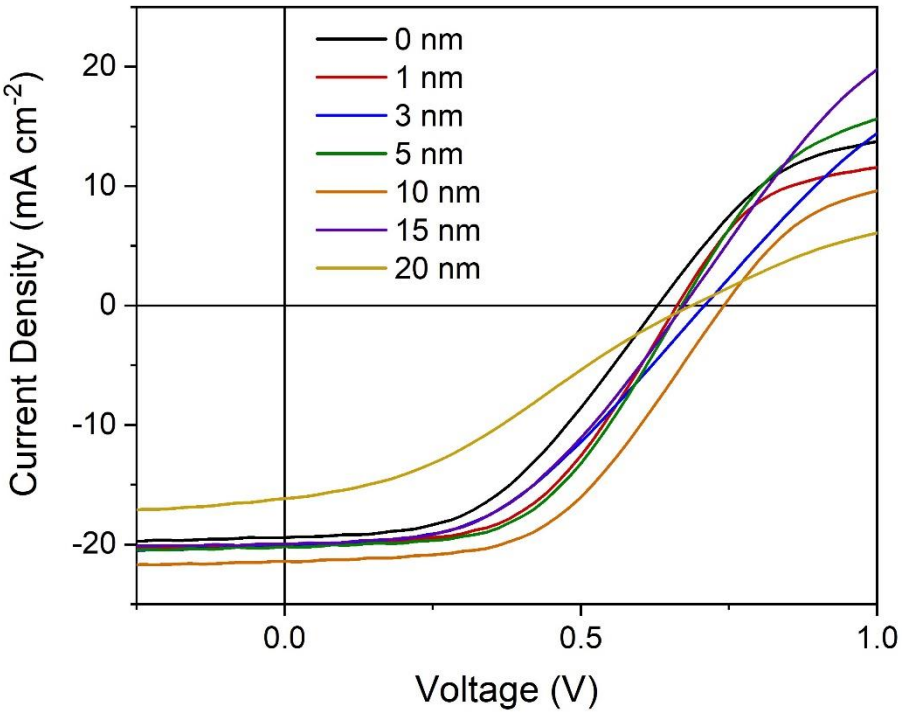

Figure 6.21: *JV* curves of the highest efficiency contacts from CdTe/SnO_2 devices with 0 – 20 nm NaF evaporated onto the back surface prior to $MgCl_2$ activation at 430°C for 20 min in air

The EQE curves for the highest efficiency contact of each device with varied NaF treatment are shown in Figure 6.22a, and are noticeably different to typical CdS/CdTe spectra due to the absence of a CdS absorption shoulder around 300 – 500 nm. The higher band gap SnO_2 allows more carriers to reach the CdTe layer and therefore improved EQE for small wavelengths. All devices show a similar EQE response regardless of NaF thickness, however there are some subtle differences. There is a minor but consistent shift in the CdTe absorption edge from 1.46 eV without NaF to 1.47 eV with NaF irrespective of thickness, which could signal a small change in stress narrowing the CdTe band gap [56]. Additionally, the collection efficiency for wavelengths between 400 – 700 nm is slightly increased for all NaF treated devices compared to the NaF free device. This contributes to an increase in the expected short circuit current density for most devices, which is calculated by the integrating the EQE curves and accounting for the AM1.5 solar spectrum, shown in Figure 6.22b as a function of NaF thickness. This shows that the short circuit current density increases with NaF thickness before a sharp decline for the 20 nm device, although the absolute variation in current density as a result of these minor changes in EQE response is minimal. Whilst this trend is qualitatively similar to the J_{sc} measured from *JV* curves, the integrated J_{sc} values from EQE measurements are significantly higher. This is because EQE measurements taken without a light bias do not probe the solar cell under the conditions it would normally operate, and can therefore overestimate J_{sc} [57]. This

effect is especially noticeable where a barrier exists at the junction interface such as for SnO_2/CdTe devices, thereby requiring carrier transport via thermionic emission.

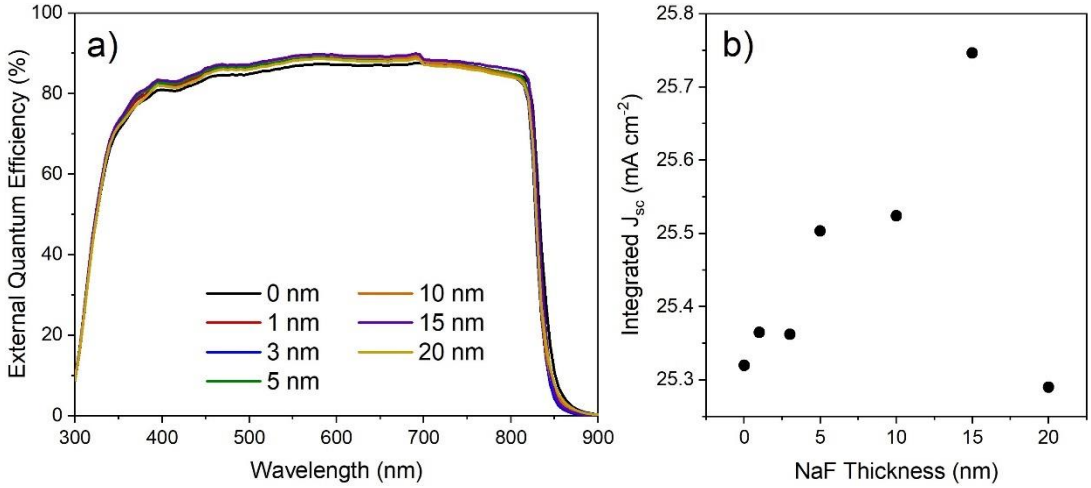

Figure 6.22: a) EQE measurements of the highest efficiency contact from CdTe/SnO_2 devices with 0-20nm NaF deposited at back surface prior to $MgCl_2$ treatment and b) short circuit current density calculated from these EQE measurements accounting for the AM1.5G spectrum

Figure 6.23 shows the acceptor density profile as well as the estimated bulk doping density and depletion width for devices with 0 – 20 nm NaF deposited before $MgCl_2$ activation. This shows that the doping density of CdTe/SnO_2 solar cells is increased by at least an order of magnitude using a combined NaF and $MgCl_2$ treatment compared to $MgCl_2$ treatment alone for all NaF thicknesses studied. This trend was not observed in CdTe/CdS devices, although it is unclear whether the true doping density is obscured in that case by limitations of the *CV* technique when applied to multiple junctions (i.e. when probing regions CdS/CdTe and SnO_2/CdTe simultaneously). The acceptor concentration is abruptly increased from 5×10^{13} cm^{-3} for a standard $MgCl_2$ treatment to a peak of 10^{15} cm^{-3} with the addition of 3 nm NaF, before stabilising at ~3×10^{14} cm^{-3} for any further NaF thicknesses. Similar behaviour is found in CdTe:Cu devices [58], whereby a small amount of copper rapidly increases doping density, with high activation ratio leading to long carrier lifetime, before excess copper atoms incorporate interstitially into the lattice and form compensating defects which lower the net doping density.

The peak doping density for 3 nm NaF would suggest that further increases beyond this would act to lower the carrier lifetime due to carrier compensation and therefore be detrimental to device performance. Whilst this is likely the case, this maximum does not match that of device efficiency nor open circuit voltage, which do not peak until 10nm NaF (note 3nm NaF device has a low fill factor, yet accounting for this does not explain continued improvements with NaF) . This indicates that compensating defects resulting from excess sodium are somewhat tolerable, and any harmful impact on device performance is outweighed by an additional

mechanism by which CdTe devices benefit from NaF in excess of the amount required for optimal doping. This could be a result of improved crystallinity due to enhanced recrystallization upon combined NaF and $MgCl_2$ treatment. Although CSS grown CdTe layers are less susceptible to recrystallization due to the high temperature deposition used, grain size is typically smaller at the interface and increases with film thickness [59]. Growth of small grains near the interface could reduce grain boundary density and therefore lower recombination. Alternatively, NaF could have a defect passivating effect similar to that for CIGS devices, where alkali post deposition treatments are far more common [60]. Whilst sodium passivation has not been experimentally proven for CdTe, recent computational studies have suggested Na preferentially segregates to grain boundaries, where it is effective in breaking the Cd-Cd double bond and removing the associated mid-gap state [61]. Further study into the behaviour of defects following NaF and $MgCl_2$ treatment is required to determine the true effect.

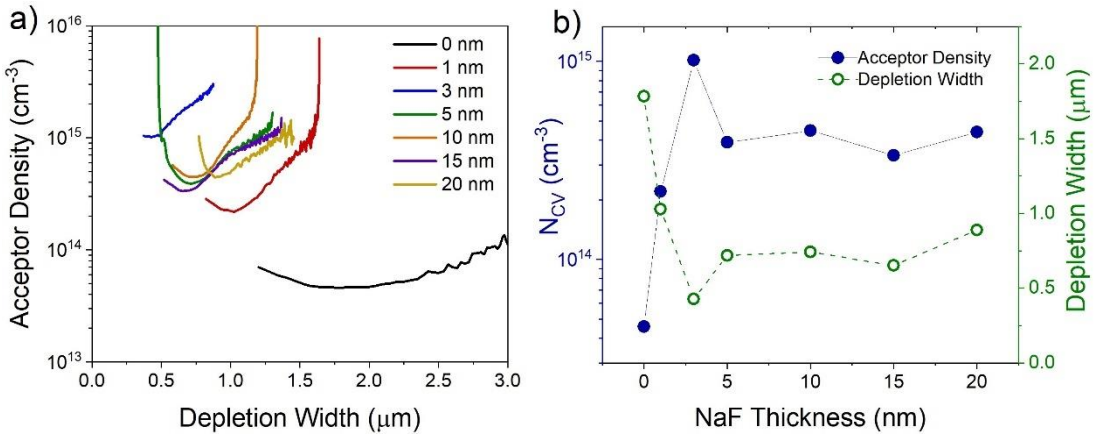

Figure 6.23: (a) Acceptor density profiles and (b) the associated bulk doping density and depletion width, calculated from *CV* measurements of for $CdTe/SnO_2$ devices with 0 – 20 nm NaF deposited prior to $MgCl_2$ activation

6.4.3 Structural Characterisation

Whilst CSS grown CdTe has been shown to be stable against recrystallization during NaF-$MgCl_2$ treatment due to the large as deposited grain size, previous attempts to incorporate this into CdTe/CdS devices were hindered by tellurium precipitation which contributed to a decrease in shunt resistance. Figure 6.24a provides XRD data for $CdTe/SnO_2$ devices incorporating 0 – 20 nm NaF during $MgCl_2$ activation, which shows there are no such Te peaks visible, with the CdTe remaining as a single phase after 20 nm NaF. This suggests that the CdS layer is vital for the reaction in which Te precipitates, either as a reactant which is consumed during the formation of elemental tellurium, or in an intermediate step which enables the reaction to take place (the highly reactivity of CdS and NaF means that CdF and NaS are likely to be available to participate in further reactions).

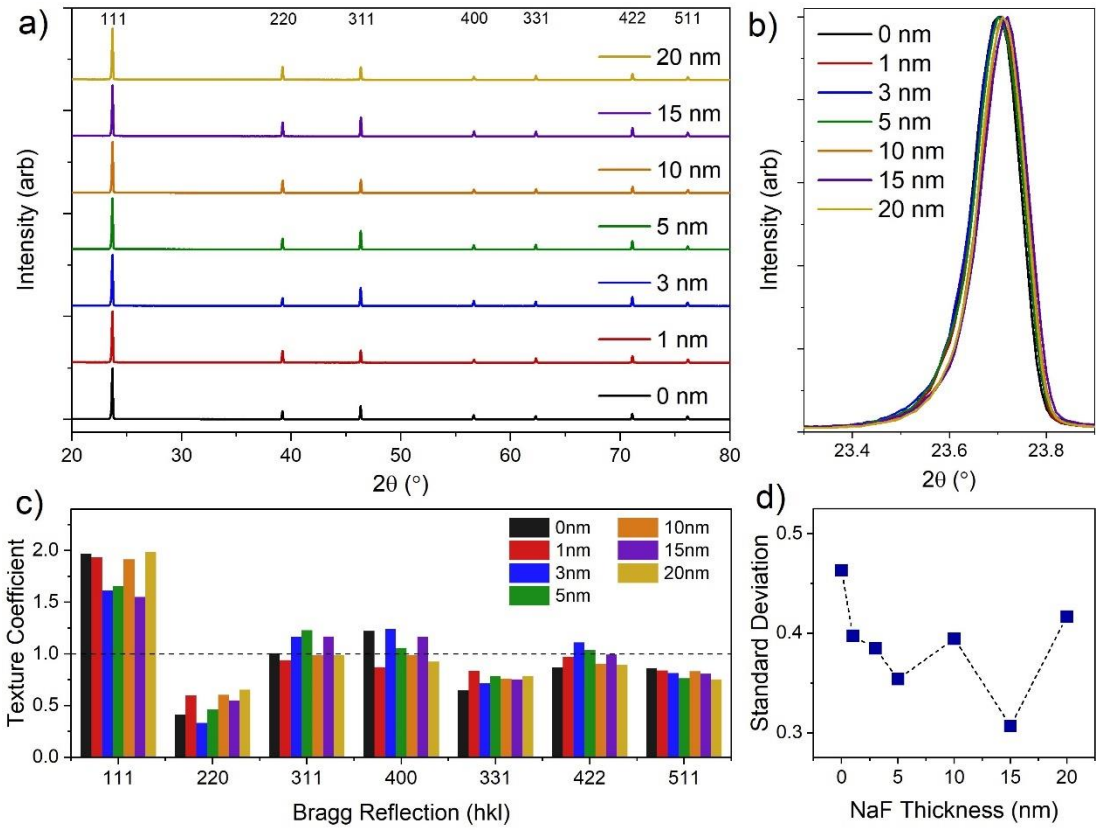

Figure 6.24: XRD data for CdTe/SnO_2 devices with 0-20nm NaF deposited prior to $MgCl_2$ treatment. (a) shows the entire spectrum collected, with the 111 peaks shown more clearly in (b). The texture coefficient for the seven CdTe reflections are given (c), as well as the standard deviation (d).

There is no sign of broadening of the 111 peak shown in Figure 6.24b, as was observed in CdS/CdTe devices in Figure 6.16, further indicating that stability of SnO_2 as a substrate. The slight asymmetric broadening seen towards lower angle is not influenced by NaF thickness. This could either be an artefact of increased counts due to a larger specimen interaction volume of material probed at low angle due to the limited penetration depth, or inhomogeneous strain causing a variation in lattice spacing as a function of CdTe thickness. Whilst the standard deviation in Figure 6.24d appears to decrease slightly for devices treated with NaF, inspection of texture coefficient for individual Bragg peaks in Figure 6.24c shows there is no consistent trend with NaF thickness and therefore changes in standard deviation are not significant.

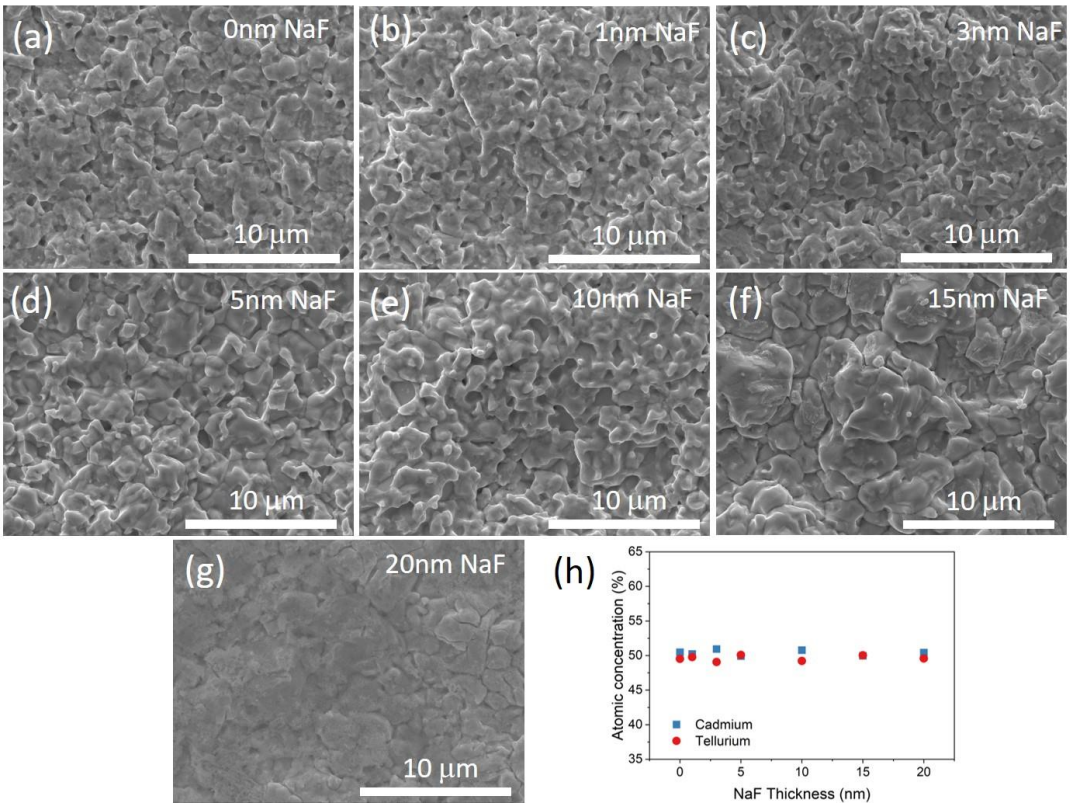

Figure 6.25: SEM images of the back surface of CdTe/SnO_2 devices with (a) 0 nm, (b) 1 nm, (c) 3 nm, (d) 5 nm, (e) 10 nm, (f) 15 nm and (g) 20 nm NaF deposited prior to $MgCl_2$ activation, as well as EDX results showing the amount of Cd and Te detected for each NaF thickness

Figure 6.25 shows micrographs of the back surface of CdTe/SnO_2 devices with different NaF thickness deposited prior to $MgCl_2$ treatment. These confirm that no significant recrystallization occurs as visible from the back surface, with continuous coverage maintained in all cases. As was the case for CdS/CdTe devices, the addition of 20 nm NaF to the $MgCl_2$ treatment resulted in sample charging during SEM imaging, producing poor quality images. Considering the increased series resistance for thick NaF layers, this highlights the requirement for further study on the removal of all oxide phases at the back surface prior to Au deposition to ensure a good quality contact. EDX results shown in Figure 6.25h indicate that all films are either stoichiometric or slightly Cd rich. The Cd/Te ratio of films grown via CSS depends on the source and substrate temperature, with higher temperature deposition producing tellurium rich films [62]. Figure 6.25h therefore indicates that a higher CdTe deposition temperature may be required to increase the tellurium content of these films, which would be expected to aid Na substitutional doping on vacant Cd sites. Neither the cadmium or tellurium concentrations vary with NaF thickness, with no sign of the Te formation and/or Cd loss that has hindered previous attempts at sodium inclusion on CdS substrates.

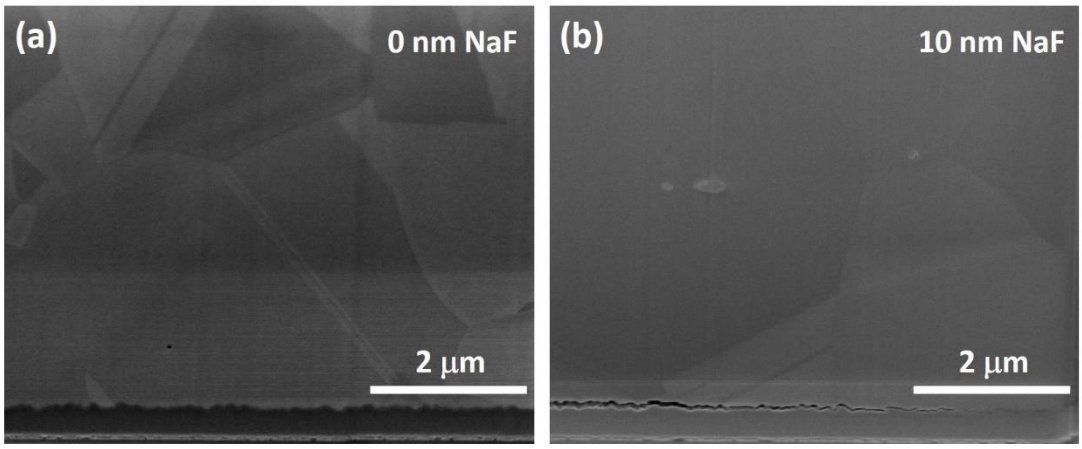

Figure 6.26: SEM images of the cross section of CdTe/SnO_2 devices with (a) 0 nm and (b) 10 nm NaF deposited at the back surface prior to $MgCl_2$ treatment

Figure 6.26 shows cross sections of CdTe/SnO_2 solar cells with a standard $MgCl_2$ activation process compared to a device with 10 nm NaF deposited prior to $MgCl_2$ activation which was found to result in the highest efficiency. In both images, the CdTe layer does not show any sign of the interfacial voids observed for CdTe/CdS devices in Figure 6.19. The SnO_2 layer is not expected to intermix with the CdTe and therefore the Kirkendall effect is suppressed, preventing the formation of the void regions and the associated efficiency loss. However, the device with combined NaF and $MgCl_2$ activation shows regions where the CdTe layer is delaminated from the SnO_2 substrate, which will severely limit device performance. Similar adhesion issues are seen in overtreated CdTe devices subject to a standard $CdCl_2$ activation [63] and therefore the addition of NaF appears to exaggerate this phenomenon.

6.4.4 Discussion

SnO_2/CdTe devices show improvement compared to standard $MgCl_2$ treated devices upon incorporation of NaF, with 10 nm resulting in the highest efficiency through improvement in all performance parameters. Whilst efficiencies for these SnO_2/CdTe devices remain lower than typical CdS device despite optimal NaF-$MgCl_2$ treatment, this work shows that using a more robust *n*-type layer together with a combined Na/Cl treatment can be more effective activation treatment than Cl alone. Therefore it is the relative efficiency increase, rather than absolute efficiency, that should be highlighted. Recent work has shown $CdSe_xTe_{1-x}/SnO_2$ devices with ~19% efficiency [53] demonstrating SnO_2 can be effective as a window layer, however the effect of NaF on selenium graded CdTe remains unclear. There is no reason to suspect this benefit is limited to CdTe deposited on SnO_2 substrates, and likely to be readily transferable to other device architectures such as MZO/CdTe and possibly MZO/$CdSe_xTe_{1-x}$.

It remains unclear what mechanism is behind the observed improvements and is likely a result of several overlapping processes. The increased doping density will certainly help, although maximum doping density does not correspond to the highest efficiency device and therefore is not the only effect. Sodium is shown to aid recrystallization of CdTe, especially for small grain material deposited at low temperature, acting as a flux in combination with chlorine. This may be caused by sodium resulting in a lower CdTe-$CdCl_2$ eutectic temperature which could aid recrystallization of stacking faults despite no observed increase in grain size increase. It is also unclear whether acceptor increase is due to Na_{Cd} substitutional doping or the passivation of compensating defects as is the case for CIGS [60]. Sodium has recently predicted to be effective in passivating defects in CdTe, especially when combined with chlorine [61]. By substitution on both the cation and anion sites with chlorine and sodium, it might be possible to move harmful defect states formed at grain boundaries by Cd and Te double bonds into the valence band and therefore these eliminate mid-gap states. Nonetheless it remains unclear which of these mechanisms is causing the efficiency improvement and may well be a contribution of all. Just as the standard $CdCl_2$ treatment has myriad of effects which occur simultaneously such as recrystallization, doping and junction formation, the addition of Na may also have several overlapping effects which are difficult to disentangle.

6.5 Conclusion

The effect of sodium on the device properties of CdTe solar cells has been studied with the addition of NaF both before and after $MgCl_2$ treatment as well as on CdS and SnO_2 substrates. By separating the NaF and $MgCl_2$ treatments, depositing 1 nm NaF immediately prior to contacting, a decrease in series and subsequent improvement in fill factor is achieved through the formation of a highly doped back surface region. This assists the formation of an ohmic contact without the requirement for further processing. In order to increase the doping density in the bulk CdTe layer, a high temperature (> 300°C) anneal is required to effectively incorporate sodium uniformly throughout the device. Below 300°C sodium diffuses rapidly, presumably via grain boundaries, and accumulates at the front contact with only a minor increase in the concentration in the bulk. Above 300°C the sodium is moved into the grain interior and increases the acceptor concentration. There is no increase in the fluorine content in any of these devices compared to a NaF-free device, suggesting that sodium is the cause of the observed effects, and consistent with previous reports which demonstrate a lack of fluorine incorporation. The high temperature anneal required to activate dopants also forms a TeO_2 oxide layer at the back surface, which increases the series resistance and partially negates the

beneficial effects of sodium incorporation, leading to only modest improvements in overall device efficiency.

Instead of incorporating sodium after chlorine activation, a series of CdTe/CdS solar cells were prepared with a combined NaF-$MgCl_2$ treatment. By maintaining a high substrate temperature during the deposition process, a large as deposited grain size was achieved for CdTe which prevents the weakening of grain boundaries observed in previous attempts. Despite this, the CdS layer is severely degraded for increasing NaF thicknesses and tellurium was found to precipitate out as secondary phases. This resulted in a strong decrease in shunt resistance and poor device performance, however suggesting that recrystallization of the CdS layer rather than CdTe is the primary issue when using a combed Na and Cl activation treatment.

Considering this, further tests were carried out by replacing the CdS *n*-type layer to form a CdTe/SnO_2 heterojunction. Although this results in a lower efficiency due to an inferior junction quality, the addition of NaF to the $MgCl_2$ treatment was found to have a beneficial effect on all device parameters, and doping density was increased by more than an order of magnitude compared to where no NaF was included. Despite minimal process optimisation, an efficiency of 8.1% was achieved with the addition of 10 nm NaF with a 110 mV increase in V_{oc} relative to a control device. Several possible mechanisms are proposed for this improvement, including Na_{Cd} substitutional doping, recrystallization of near-interface small grains, and Na induced passivation of Cd double bonds at grain boundaries.

Further work in this area should focus on the design of an improved and more targeted activation treatment, possibly combining NaCl with $MgCl_2$ to eliminate any effect of fluorine may have and result in a simpler defect structure. The effect of other alkali metals is also of interest, either alone or in combination with sodium as is optimal for the post deposition treatment of CIGS devices. It has been shown that Na, which is common impurity in CdTe, can have beneficial effect on device performance. However, rather than relying on uncontrolled diffusion from the glass substrate, or its presence in raw material, it should be introduced in a controlled manner to maximise benefit. It may be that the benefit of Na is underreported here since control devices already have a significant amount of sodium as an unintentional impurity, and therefore comparing to more highly pure material deposited on alkali free substrates might confirm this. Improvements to the device structure reported here should focus on confirming that the fill factor loss can be attributed to an oxidised back contact layer, and then on alternative etchants to remove this to realise the full benefit of NaF/$MgCl_2$ treatment.

6.6 References

1. Hand, R. J. & Tadjiev, D. R. Mechanical properties of silicate glasses as a function of composition. in *Journal of Non-Crystalline Solids* vol. 356 2417–2423 (North-Holland, 2010).
2. Yan, Y. *et al.* SiO2 as barrier layer for Na out-diffusion from soda-lime glass. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 2519–2521 (2010).
3. Major, J. D., Bowen, L. & Durose, K. Focussed ion beam and field emission gun-scanning electron microscopy for the investigation of voiding and interface phenomena in thin-film solar cells. *Progress in Photovoltaics: Research and Applications* **20**, 892–898 (2012).
4. Kranz, L. *et al.* Effect of sodium on recrystallization and photovoltaic properties of CdTe solar cells. *Solar Energy Materials and Solar Cells* **105**, 213–219 (2012).
5. Durose, K. *et al.* The influence of NaCl on the microstructure of CdS films and CdTe solar cells. in *Microscopy of Semiconductor Materials* 207–210 (1999).
6. Wei, S.-H. & Zhang, S. B. Chemical trends of defect formation and doping limit in II-VI semiconductors: The case of CdTe. *Physical Review B* **66**, 155211 (2002).
7. Amirkhalili, A., Barrioz, V., Irvine, S. J. C., Beattie, N. S. & Zoppi, G. A combined Na and Cl treatment to promote grain growth in MOCVD grown CdTe thin films. *Journal of Alloys and Compounds* **699**, 969–975 (2017).
8. Dhere, R. *et al.* Effect of Na incorporation on the growth and properties of CdTe/CdS devices. in *Conference Record of the Thirty-first IEEE* 279–282 (2005).
9. Perrenoud, J. *et al.* A comprehensive picture of Cu doping in CdTe solar cells. *Journal of Applied Physics* **114**, 174505 (2013).
10. Yang, J. H., Metzger, W. K. & Wei, S. H. Carrier providers or killers: The case of Cu defects in CdTe. *Applied Physics Letters* **111**, 042106 (2017).
11. Hegedus, S. S., McCandless, B. E. & Birkmire, R. W. Analysis of stress-induced degradation in CdS/CdTe solar cells. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 535–538 (2000).
12. Kanevce, A. & Gessert, T. A. Optimizing CdTe solar cell performance: Impact of variations in minority-carrier lifetime and carrier density profile. *IEEE Journal of Photovoltaics* **1**, 99–103 (2011).
13. Emziane, M., Durose, K., Romeo, N., Bosio, A. & Halliday, D. P. A combined SIMS and ICPMS investigation of the origin and distribution of potentially electrically active impurities in CdTe/CdS solar cell structures. *Semiconductor Science and Technology* **20**, 434 (2005).
14. Halliday, D. P., Emziane, M., Durose, K., Bosio, A. & Romeo, N. Effects of impurities in CdTe/CdS structures: Towards enhanced device efficiencies. in *Conference Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion, WCPEC-4* vol. 1 408–411 (2006).
15. Durose, K., Cousins, M. A., Boyle, D. S., Beier, J. & Bonnet, D. Grain boundaries and impurities in CdTe/CdS solar cells. in *Thin Solid Films* vols. 403–404 396–404 (Elsevier, 2002).

16. Akis, R. *et al.* Extracting Cu diffusion parameters in polycrystalline CdTe. in *2014 IEEE 40th Photovoltaic Specialist Conference, PVSC 2014* 3276–3281 (Institute of Electrical and Electronics Engineers Inc., 2014). doi:10.1109/PVSC.2014.6925635.

17. Chou, H. C., Rohatgi, A., Jokerst, N. M., Thomas, E. W. & Kamra, S. Copper migration in CdTe heterojunction solar cells. *Journal of Electronic Materials* **25**, 1093–1098 (1996).

18. Poplawsky, J. D. *et al.* Nanoscale doping profiles within CdTe grain boundaries and at the CdS/CdTe interface revealed by atom probe tomography and STEM EBIC. *Solar Energy Materials and Solar Cells* **150**, 95–101 (2016).

19. Hofmann, D. M. *et al.* Identification of the chlorine A-center in CdTe. *Physical Review B* **45**, 6247–6250 (1992).

20. Romeo, N., Bosio, A., Canevari, V. & Podestà, A. Recent progress on CdTe/CdS thin film solar cells. *Solar Energy* **77**, 795–801 (2004).

21. Mazzamuto, S. *et al.* A study of the CdTe treatment with a Freon gas such as CHF_2Cl. *Thin Solid Films* **516**, 7079–7083 (2008).

22. Laemmle, A. *et al.* Investigation of the diffusion behavior of sodium in Cu(In,Ga)Se 2 layers. *Journal of Applied Physics* **115**, (2014).

23. Emziane, M., Durose, K., Halliday, D. P., Romeo, N. & Bosio, A. SIMS depth profiling of CdTe-based solar cells grown on sapphire substrates. *Thin Solid Films* **511–512**, 66–70 (2006).

24. Zinner, E. Depth profiling by secondary ion mass spectrometry. *Scanning* **3**, 57–78 (1980).

25. Singh, V. P., Erickson, O. M. & Chao, J. H. Analysis of contact degradation at the CdTe-electrode interface in thin film CdTe-CdS solar cells. *Journal of Applied Physics* **78**, 4538–4542 (1995).

26. Reese, M. O. *et al.* Surface passivation of CdTe single crystals. *IEEE Journal of Photovoltaics* **5**, 382–385 (2015).

27. Yang, J.-H., Yin, W.-J., Park, J.-S., Ma, J. & Wei, S.-H. Review on first-principles study of defect properties of CdTe as a solar cell absorber. *Semiconductor Science and Technology* **31**, 083002 (2016).

28. Metzger, W. K. *et al.* Time-resolved photoluminescence studies of CdTe solar cells. *Journal of Applied Physics* **94**, 3549–3555 (2003).

29. Metzger, W. K., Ahrenkiel, R. K., Dashdorj, J. & Friedman, D. J. Analysis of charge separation dynamics in a semiconductor junction. *Physical Review B - Condensed Matter and Materials Physics* **71**, 035301 (2005).

30. Duenow, J. N. *et al.* Single-crystal CdTe solar cells with V_{oc} greater than 900 mV. *Applied Physics Letters* **105**, 053903 (2014).

31. Perrenoud, J. *et al.* A comprehensive picture of Cu doping in CdTe solar cells. *Journal of Applied Physics* **114**, 174505 (2013).

32. Moutinho, H. R. *et al.* Studies of recrystallization of CdTe thin films after CdCl/sub 2/ treatment. in 431–434 (Institute of Electrical and Electronics Engineers (IEEE), 2002). doi:10.1109/pvsc.1997.654120.

33. Taylor, A. A. *et al.* A comparative study of microstructural stability and sulphur diffusion in CdS/CdTe photovoltaic devices. *Solar Energy Materials and Solar Cells* **141**, 341–349 (2015).

34. Papageorgiou, G. Nano-and Micro-structured CdTe Solar Cells. (University of Liverpool, 2018).

35. Jensen, S. A. *et al.* Long carrier lifetimes in large-grain polycrystalline CdTe without $CdCl_2$. *Journal of Applied Physics* **108**, 263903–214506 (2016).

36. Major, J. D. & Durose, K. Early stage growth mechanisms of CdTe thin films deposited by close space sublimation for solar cells. *Solar Energy Materials and Solar Cells* **95**, 3165–3170 (2011).

37. Kaminski, P. M. *et al.* Internal strain analysis of CdTe thin films deposited by pulsed DC magnetron sputtering. in *2015 IEEE 42nd Photovoltaic Specialist Conference, PVSC 2015* (Institute of Electrical and Electronics Engineers Inc., 2015). doi:10.1109/PVSC.2015.7356093.

38. Emziane, M., Durose, K., Halliday, D. P., Romeo, N. & Bosio, A. SIMS depth profiling of CdTe-based solar cells grown on sapphire substrates. *Thin Solid Films* **511–512**, 66–70 (2006).

39. Williams, B. L. *et al.* A Comparative Study of the Effects of Nontoxic Chloride Treatments on CdTe Solar Cell Microstructure and Stoichiometry. *Advanced Energy Materials* **5**, 1500554 (2015).

40. Tai, H. & Hori, S. Equilibrium Phase Diagrams of the CdTe-$CdCl_2$ and CdTe-$CdBr_2$ Systems. *Nippon Kinzoku Gakkaishi/Journal of the Japan Institute of Metals* **40**, 722–725 (1976).

41. Hegedus, S., Desai, D. & Thompson, C. Voltage dependent photocurrent collection in CdTe/CdS solar cells. *Progress in Photovoltaics: Research and Applications* **15**, 587–602 (2007).

42. Demtsu, S. H. & Sites, J. R. Quantification of losses in thin-film CdS/CdTe solar cells. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 347–350 (2005).

43. Baines, T. *et al.* Incorporation of CdSe layers into CdTe thin film solar cells. *Solar Energy Materials and Solar Cells* **180**, 196–204 (2018).

44. McCandless, B. E., Engelmann, M. G. & Birkmire, R. W. Interdiffusion of CdS/CdTe thin films: Modeling x-ray diffraction line profiles. *Journal of Applied Physics* **89**, 988–994 (2001).

45. Li, J. V. *et al.* Theoretical analysis of effects of deep level, back contact, and absorber thickness on capacitance-voltage profiling of CdTe thin-film solar cells. *Solar Energy Materials and Solar Cells* **100**, 126–131 (2012).

46. Haendler, H. M. & Bernard, W. J. The Reaction of Fluorine with Cadmium and Some of its Binary Compounds. The Crystal Structure, Density and Melting Point of Cadmium Fluoride. *Journal of the American Chemical Society* **73**, 5218–5219 (1951).

47. Shin, S. H., Bajaj, J., Moudy, L. A. & Cheung, D. T. Characterization of Te precipitates in CdTe crystals. *Applied Physics Letters* **43**, 68–70 (1983).

48. Misra, S. *et al.* Cadmium Selective Etching in CdTe Solar Cells Produces Detrimental Narrow-Gap Te in Grain Boundaries. *ACS Applied Energy Materials* **3**, 1749–1758 (2020).

49. Major, J. D., Bowen, L., Treharne, R. & Durose, K. Assessment of photovoltaic junction position using combined focused ion beam and electron beam-induced current analysis of close space sublimation deposited CdTe solar cells. *Progress in Photovoltaics: Research and Applications* **22**, 1096–1104 (2014).

50. Abbas, A. *et al.* The effect of cadmium chloride treatment on close-spaced sublimated cadmium telluride thin-film solar cells. *IEEE Journal of Photovoltaics* **3**, 1361–1366 (2013).

51. Yoo, S. H. *et al.* Identification of critical stacking faults in thin-film CdTe solar cells. *Applied Physics Letters* **105**, 062104 (2014).

52. Kephart, J. M. *et al.* Band alignment of front contact layers for high-efficiency CdTe solar cells. *Solar Energy Materials and Solar Cells* **157**, 266–275 (2016).

53. Ablekim, T. *et al.* Thin-Film Solar Cells with 19% Efficiency by Thermal Evaporation of CdSe and CdTe. *ACS Energy Letters* **5**, 892–896 (2020).

54. Munshi, A. H. *et al.* Polycrystalline CdTe photovoltaics with efficiency over 18% through improved absorber passivation and current collection. *Solar Energy Materials and Solar Cells* **176**, 9–18 (2018).

55. Li, D. B. *et al.* Eliminating S-kink to maximize the performance of MgZnO/CdTe solar cells. *ACS Applied Energy Materials* **2**, 2896–2903 (2019).

56. Rindner, W. & Pittelli, E. Effects of stress-induced band-gap widening and defects in GaAs junctions. *Journal of Applied Physics* **37**, 4437–4439 (1966).

57. Scheer, R. & Schock, H.-W. Appendix A: Frequently Observed Anomalies. in *Chalcogenide Photovoltaics* 305–314 (Wiley-VCH Verlag GmbH & Co. KGaA, 2011). doi:10.1002/9783527633708.ch7.

58. Kranz, L. *et al.* Doping of polycrystalline CdTe for high-efficiency solar cells on flexible metal foil. *Nature Communications* **4**, 1–7 (2013).

59. Durose, K., Cousins, M. A., Boyle, D. S., Beier, J. & Bonnet, D. Grain boundaries and impurities in CdTe/CdS solar cells. in *Thin Solid Films* vols. 403–404 396–404 (Elsevier, 2002).

60. Reinhard, P. *et al.* Features of KF and NaF Postdeposition Treatments of Cu(In,Ga)Se2 Absorbers for High Efficiency Thin Film Solar Cells. *Chemistry of Materials* **27**, 5755–5764 (2015).

61. Tong, C. J. & McKenna, K. P. Passivating grain boundaries in polycrystalline CdTe. *Journal of Physical Chemistry C* **123**, 23882–23889 (2019).

62. Greenberg, J. H. P-T-X phase equilibrium and vapor pressure scanning of non-stoichiometry in CdTe. *Journal of Crystal Growth* **161**, 1–11 (1996).

63. Wu, X. *et al.* High-efficiency $Cd_2SnO_4/Zn_2SnO_4/Zn_xCd_{1-x}S$/CdS/CdTe polycrystalline thin-film solar cells. in *Conference Record of the IEEE Photovoltaic Specialists Conference* 470–474 (2000).

Chapter 7

Growth and optimisation of CdTe solar cells on alternative window layers

7.1 Introduction

CdTe solar cells have historically been based on a heterojunction with CdS, since a homojunction is not feasible due to a strong absorption coefficient resulting in a shallow junction close to a highly defective surface [1]. Until recently this architecture had not significantly changed for around 40 years, despite the relatively low band gap of CdS resulting in parasitic absorption which limits the available current output from devices. To avoid this, several strategies have been employed to increase the amount of light reaching the CdTe layer, where the majority of the electric field resides and electron-hole pairs can be effectively separated. Alloying CdS with higher band gap materials such as ZnS allows the band gap to be varied between 2.4 and 3.6 eV which enables some improvement in the blue response, however this is accompanied by an increased resistivity and for $Cd_{1-x}Zn_xS$ compositions with band gaps above 3 eV performance deteriorates rapidly [2]. Simply reducing the thickness of the CdS layer can be effective to some extent, although this is limited by the requirement for a pinhole free film that is not consumed by interdiffusion during the subsequent processing steps[3]. The use of a high resistivity transparent (HRT) buffer layer allows for thinner CdS to be used, whilst maintaining V_{oc} and fill factor [4]. Combining a suitable HRT layer with a nanostructured CdS:O film, which can controllably increase the CdS band gap [5] , improves current collection, although this is also accompanied by increased series resistance [6].

Recent insights into the importance of band alignment have allowed the CdS layer to be eliminated entirely, and replaced with a ZnO layer alloyed with MgO (MZO) to vary the band gap thereby tuning the conduction band offset to optimise transport across the interface [4].

Depositing CdTe onto MZO substrates has enabled higher efficiencies due to increased current density, although careful process control is required to prevent a secondary barrier at the front contact causing abnormal *JV* curves which severely lowers fill factor [7]. Different processing strategies have emerged amongst various research groups to prevent this 'S' shaped curve such as limiting the layer thickness [4], reducing the oxygen content [7], varying the Mg/Zn ratio [8] and post growth annealing [9]. This strong sensitivity to processing conditions as well as indications of degradation due to the MgO content in MZO films reacting with water vapour [10], mean that other alternative partner layers remain worthy of investigation.

SnO_2 is investigated here in comparison to CdS as an alternative window layer on which to grow CdTe. The widespread use of FTO as the front contact for CdTe PV devices means SnO_2 based HRT layers are a natural choice, with HRT/FTO bilayers perhaps offering favourable interface properties as well as being attractive from a manufacturing perspective. Indeed, such bilayer films are already commercially available and offer a consistent substrate on which to develop CdTe devices. Devices with a graded $CdSe_xTe_{1-x}$ absorber layer forming a junction with SnO_2 have recently shown high efficiency [11], demonstrating this as a suitable substrate on which to grow CdTe based devices.

This work examines the limitations of CdS as a window layer for CdTe solar cells in section 7.2, and investigates the use of the SnO_2 as a potential replacement in section 7.3. As well as being more transparent, this window layer is more thermally stable therefore opens the new parameter space to explore using higher temperature growth methods and/or post deposition treatments. Finally, a selenium graded absorber layer combined with a SnO_2 window layer is investigated in section 7.4.

7.2 CdTe solar cells with a CdS window layer

7.2.1 Introduction

The use of a CdS window layer in superstrate CdTe photovoltaic devices limits the thermal budget available for device processing due to the intermixing and eventual consumption of the CdS layer that can occur both during deposition [12] and chlorine activation [13]. Deposition conditions have been shown to strongly affect the crystallinity and grain structure of CdTe films, which can have a considerable impact on device performance [14,15], however the CdTe/CdS device architecture restricts the CdTe deposition conditions to those which maintain a continuous CdS layer. This is undesirable since high deposition temperatures, which are associated with large grains and therefore improved performance [16], will also cause deterioration of the CdS layer. Similarly, the optimal chlorine treatment for a device may be limited by the CdS diffusion rather than the CdTe layer itself.

In an effort to understand the limitations of the CdS/CdTe architecture and the effect of thermal history on device performance, the impact of both CdTe deposition time and $MgCl_2$ treatment temperature is examined in this section.

7.2.2 Device fabrication

TEC15 glass substrates, which include a SnO_2:F TCO layer, were coated with 100 nm CdS via sputtering at a substrate temperature of 200°C and power density of 1.32 W cm^{-2} under 5 mTorr Ar for 30 min. CdTe was then deposited by CSS onto a series of seven 5×5 cm^2 samples at different nitrogen pressure between 5 – 400 Torr, with source and substrate temperature at 650°C and 550°C respectively. By varying the pressure during CSS deposition, the adatom arrival rate can be altered [17] and therefore the CdTe growth rate can be controlled [15], with higher pressure slowing growth. For each deposition pressure the total growth time is adjusted to achieve a constant thickness of 7 μm, thereby subjecting the substrate to elevated temperature for between 4 – 162 min as shown in Table 7.2. It should be noted that the growth time does not account for the time taken for the substrate to reach and stabilise at deposition temperature and cool down to room temperature, which remains constant for all samples.

Table 7.2: CdTe growth time for TEC15/CdS/CdTe devices deposited between 5 – 400 Torr

Pressure (Torr)	**Growth Rate (μm min^{-1})**	**Growth Time (min)**
5	1.60	4.4
20	0.55	13

50	0.31	22
100	0.19	37
200	0.07	98
300	0.05	138
400	0.04	162

7.2.3 Structural analysis of CdTe films deposited on CdS at varied pressure

Figure 7.1: SEM images of the back surface of as grown CdTe films deposited on CdS at pressures between 5 – 400 Torr (a) – (g) with the grain size distribution shown inset, as well as the mean radius plotted as a function of deposition pressure (h)Figure 7.1 shows SEM images of as-deposited CdTe films deposited at pressure between 5 – 400 Torr (a) – (g), as well as the average grain radius plotted as a function of deposition pressure (h). The figure also shows histograms of the grain sizes each fitted to a gamma distribution. For low growth pressures, especially 5 Torr, there are distinct hexagonal crystal facets consistent with (111) planes bounded by <110> directions at their six edges. This is consistent with the close packed (111) planes dominating the preferred orientation, as is shown in XRD measurements in Figure 7.2. As the pressure increases, the grain shape becomes more irregular as other orientations become more prominent whilst the grains increase in size. The grain size (as determined by the radius of a circle with equivalent area) initially follows a symmetric, narrow distribution at low pressures. At higher growth pressures the distribution becomes skewed towards larger grains, accompanied by an increase in the standard deviation. There is an increase in average grain radius as shown in Figure 7.1h which levels out above 300 Torr, demonstrating that the grain size can be effectively controlled by altering the nucleation conditions via the nitrogen pressure. However, this change is much less apparent than was shown previously in a similar investigation [15]. The inclusion of oxygen in either the CdS layer or CdTe layer has proven essential for high efficiency devices deposited via CSS and strongly influences growth [18,19]. For devices grown in this work, this is achieved through careful pre-treatment of new CdTe source material by heating in an oxygen ambient. This results in high efficiency devices whilst avoiding gradual oxidation that would result from inclusion in the deposition ambient. However, oxygen is known to strongly increase the nucleation density of islands at the early stages of CdTe growth, with an oxide surface at crystallite surfaces resulting in a barrier to liquid-like coalescence of islands [20]. This stabilises grain boundaries against coalescence since this oxidised interface is maintained as islands merge, decreasing the grain size of the resulting film [21]. This can explain the discrepancy between the strength of the previously reported relationship between growth pressure and grain size [15], which did not use pre-oxidised CdTe source material. Similarly, a reduction in faceting is expected from

upon oxygen inclusion, which interrupts the step-flow mechanism by which crystal facets grow [21].

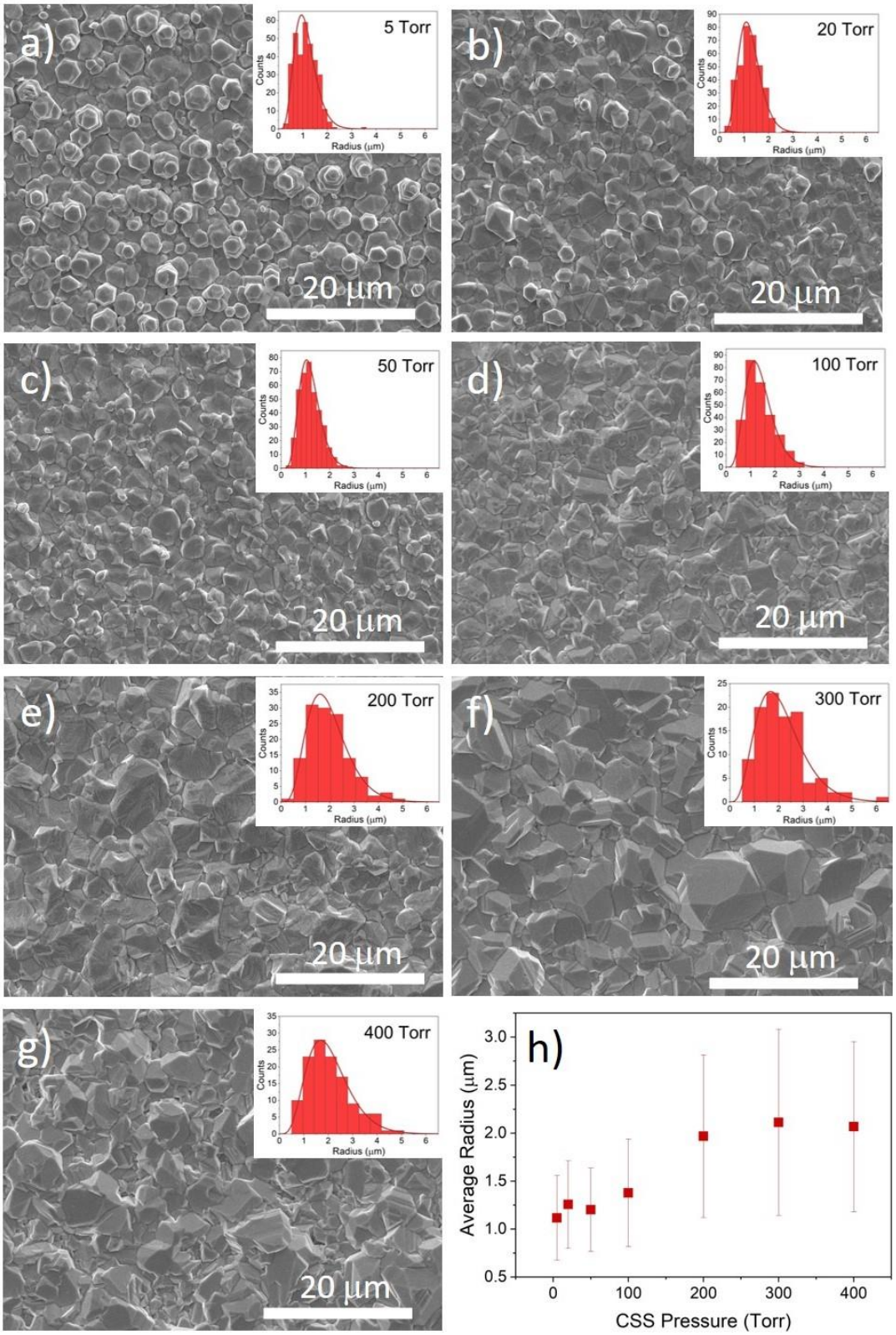

Figure 7.1: SEM images of the back surface of as grown CdTe films deposited on CdS at pressures between 5 – 400 Torr (a) – (g) with the grain size distribution shown inset, as well as the mean radius plotted as a function of deposition pressure (h)

Figure 7.2a shows θ-2θ XRD spectra for the series of samples described in section 7.2.2. All films are strongly [111] oriented, especially samples grown at lower deposition pressures. The 5 Torr samples shows only minor contributions from other peaks, which is consistent with observations from Figure 7.1a. The 111 peak for each growth pressure is shown at higher magnification in Figure 7.2b, where there is a clear asymmetry in peak shape for all samples. This is most apparent for the sample deposited at 5 Torr whereby the 111 peak is significantly broader than for other samples, with a widened shoulder towards the low angle side of the peak. Several mechanisms could possibly contribute to this asymmetric peak such as crystallite size, lattice strain and intermixing of the CdS and CdTe layers. However, since peak broadening due to crystallite size is dominant for much smaller (<100 nm) grain sizes than those involved here, and sulphur interdiffusion would be expected to decrease the lattice spacing and therefore increase the diffraction angle, inhomogeneous lattice strain appears to be the most likely cause of the observed peak broadening. In-plane compressive strain is expected at the CdS-CdTe interface due to the smaller lattice constant of CdS, which increases the lattice spacing parallel to the interface according to Poisson's ratio. Therefore this region of increased lattice spacing could contribute to the low-angle shoulder of the 111 peaks. This would be most apparent for low pressure growth whereby rapid deposition and less intermixing maintains this interfacial strain, causing the enhanced broadening seen for the 5 Torr sample. The peak shape for higher growth pressures is more consistent, with no change in FWHM and less obvious asymmetry. The peak maxima follow a pattern of increasing diffraction angle with growth pressure, with a small reversal of the trend for 5 Torr and 400 Torr. This indicates a decrease of lattice constant from 6.55Å to 6.53Å, presumably due to sulphur diffusion [3].

Figure 7.2c shows the texture coefficient for each Bragg direction as a function of deposition pressure, whereby a texture coefficient of 1 corresponds to the peak intensity expected for a randomly oriented film. At higher growth pressures, the reflections from crystallographic planes other than 111 gradually increase, indicating a more randomised texture. The intensities from the 220, 311 and 331 planes increase as the preferential orientation of the 111 plane is reduced. In contrast, the 400 and 422 orientations appear to be relatively insensitive to the growth pressure showing no trend whilst the texture coefficient for the 511 orientation decreases, with progressively lower counts than would be expected for a powder diffraction pattern. This is presumably because {511} is the $\sum = 3$ twin orientation to {111} in the zinc-blende lattice, and therefore the 511 intensity follows the same decreasing trend as the 111 peak intensity [22]. Despite this decrease for the 511 orientation, the standard deviation decreases rapidly with growth pressure indicating a more randomised texture as shown in Figure 7.2d. This is dominated by a decrease in the 111 texture coefficient, and can be attributed to the

change in growth pressure altering the nucleation density during the early stage of CdTe film formation [15]. Islands nucleate with random orientations, with dense crystallographic orientations such as the (111) plane growing quicker than others. At low pressure, the high density of nucleation sites means the larger (111) orientated islands interact with and outgrow the slower growing orientations, resulting in a strong preferential orientation. Higher growth pressure lowers the nucleation density, thereby limiting interactions between islands and allowing the original random orientation of the islands to be preserved during film growth.

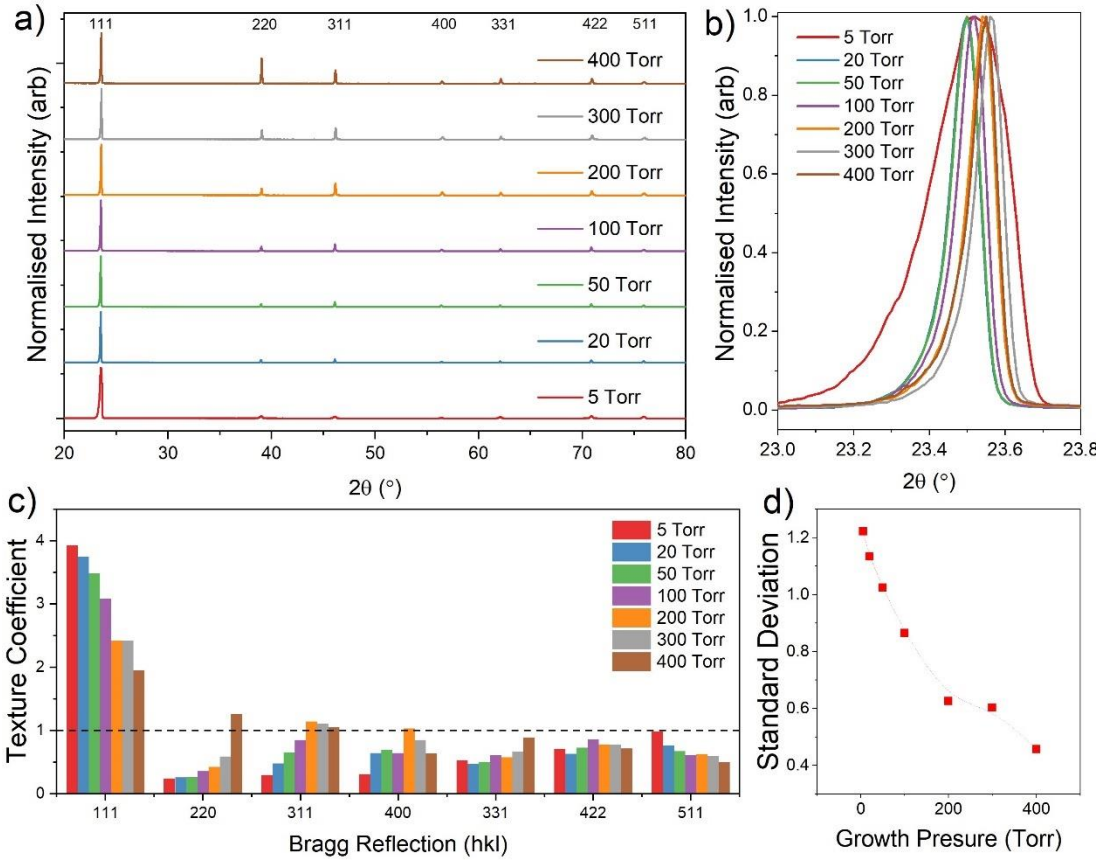

Figure 7.2: XRD data for 7 μm CdTe films grown on CdS coated substrates under varying pressure of nitrogen (a), with higher magnification of the 111 peak shown in (b). The texture coefficient for each Bragg reflection at each growth pressure is given in (c) and their standard deviation in (d)

7.2.4 Device analysis of CdTe/CdS solar cells deposited at varied pressure

A series of solar cells were processed from the films grown with varied pressure. Since device efficiency is sensitive to even small changes in temperature during the activation treatment, the $MgCl_2$ temperature was also varied between 410 – 430°C for each sample. The results are given in Figure 7.3, which show box plots of the performance parameters from devices with nine cells for each combination of growth pressure and $MgCl_2$ temperature. The efficiency of devices gradually increases with higher pressure before showing a clear peak for all treatment

temperatures at 50 Torr, after which performance deteriorates rapidly. Devices grown at 400 Torr show virtually no photovoltaic performance, and only a very weak diode response. At 410°C the open circuit voltage is not significantly changed for growth pressures up to 50 Torr after which is begins to decrease, whereas for 420°C and 430°C there is gradually more of a dependence on growth pressure below 50 Torr. Similarly the short circuit current density is not detrimentally affected by growth pressure for the 410°C series, excluding the 400 Torr sample, instead showing a small increase at higher pressure likely due to a thinner CdS layer consumed during longer growth runs. At the higher activation temperature of 430°C, the devices appear overtreated, showing lower efficiencies overall and a stronger dependence on growth pressure which peaks at 50 Torr. The series resistance initially decreases with growth pressure which could be due to the modest increase in grain size resulting in fewer grain boundaries or could be due to better interfacial properties with longer depositions which accompanies the high pressure growth. However, since the series resistance begins to increase at pressures >100 Torr despite the larger grain size for these films as shown in Figure 7.1h, grain size is not expected to be the dominant effect. Shunt resistance is decreased significantly for high growth pressures, as well as for 430°C activation treatments. This could be due to the consumption of the CdS layer during growth meaning there is effectively no *n*-type partner layer with which to form a heterojunction, or due to an increased surface roughness which is expected to accompany a larger grain size, resulting in thinner absorber areas leading to pathways for current to short circuit the device.

The efficiency of devices is highly sensitive to the activation treatment, showing a significant decrease in efficiency for only 20°C increase in temperature due to overtreatment. Chlorine is essential in removing stacking faults and planar defects in as deposited CdTe, and higher treatment temperatures have shown continuous improvement in the CdTe microstructure. This however is accompanied by an increase in concentration of chlorine at the CdS-CdTe and CdS-FTO interface, which overall proves detrimental to device performance [23]. Although a larger grain size might be expected to inhibit grain boundary assisted transport of chlorine to the front interface, no evidence of this is observed here. Shunt resistance appears to be most strongly affected by overtreatment in this case, likely a result of excess chlorine at the CdS-CdTe interface having a detrimental effect on the heterojunction. This reduces the built-in voltage which is consistent with voltage dependent collection as well as lowering of open circuit voltage and short circuit current. This demonstrates that the CdS-CdTe heterojunction limits both the $MgCl_2$ treatment temperature as well as the duration of the high temperature deposition, with deterioration of performance in both cases outside of a small window of processing conditions.

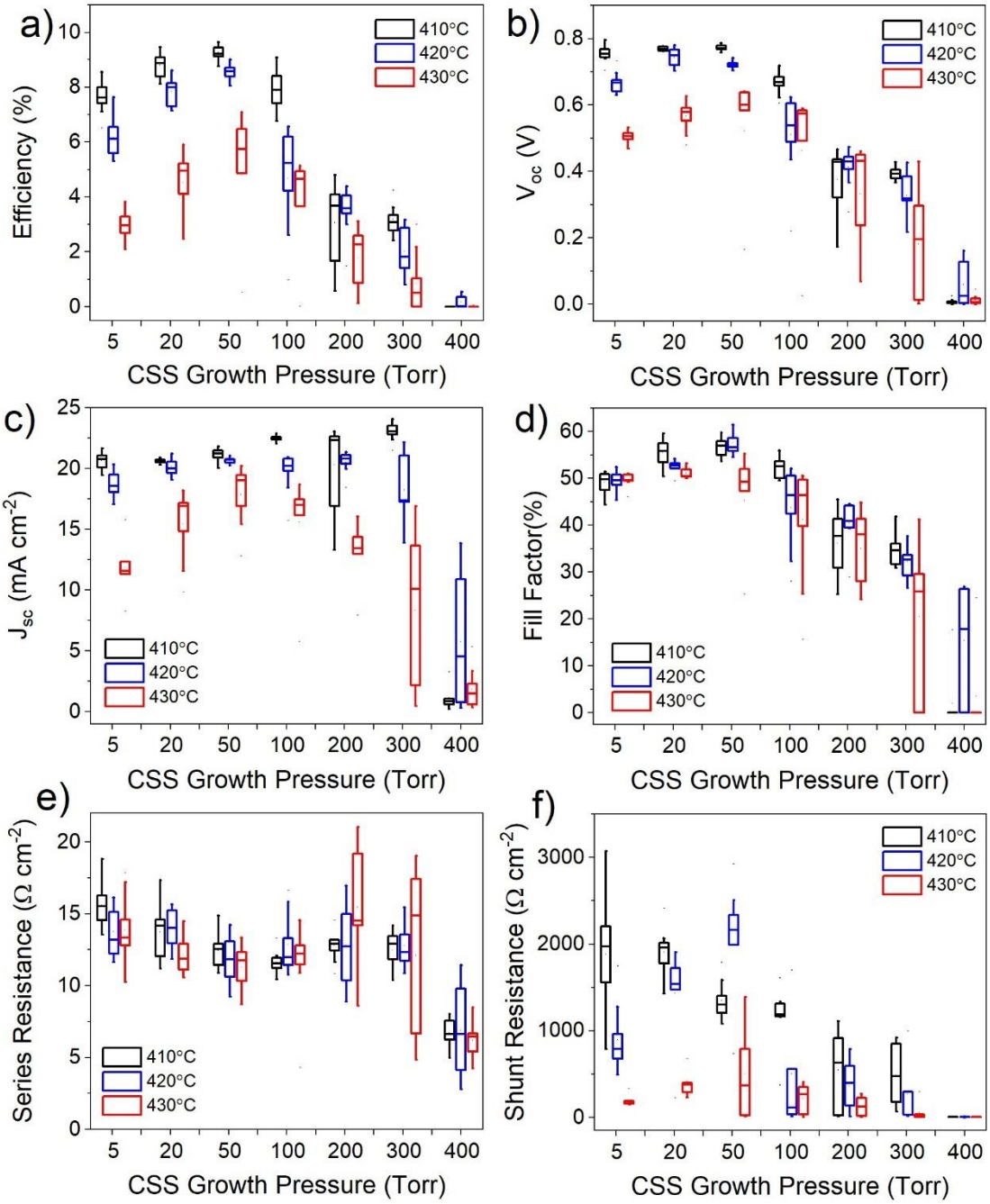

Figure 7.3: Box and whisker plots showing *JV* performance parameters for CdS/CdTe devices grown under 5 - 400 Torr of nitrogen, activated at 410°C, 420°C, 430°C. The box boundaries show the upper and lower quartiles with a horizontal line for the median value, and the range given by the whiskers. The efficiency (a), open circuit voltage (b), short circuit current density (c), fill factor (d), series resistance (e) and shunt resistance (f) is given as a function of growth pressure

Figure 7.4 shows *JV* curves corresponding to the highest efficiency contact from the series shown in Figure 7.3, comparing the effect of CdTe growth pressure on devices treated at 410°C, 420°C and 430°C. For all treatment temperatures, there is a clear difference between the shape of *JV* curves for devices grown at low and high pressure. Low pressure growth (i.e. below ~100 Torr) results in a typical *JV* response for CdTe devices, with a clear turn-on

voltage, open circuit voltage between 0.7 – 0.8 V and rollover at higher forward bias due to the effect of a back contact barrier. Rollover is expected for these devices, which have no intentional copper doped region or other contact layers that would otherwise reduce the barrier height in an effort to minimise process variables. As the growth pressure is increased above 100 Torr, a rapid drop in V_{oc} is accompanied by a much more severe rollover effect. This is likely due to a deterioration of the CdS-CdTe junction either due to intermixing of the two layers during the longer growth duration required for high pressure growth, or the resulting large grain structure offering leakage paths due to increased surface roughness. In any case, a weakened CdS-CdTe junction will be more susceptible to rollover as the back contact barrier will dominate the main junction at lower forward bias, therefore showing enhanced current blocking behaviour. For devices grown at 400 Torr, the *JV* response is almost entirely linear, showing no diode-like behaviour for all $MgCl_2$ treatment temperatures and barely entering into the fourth quadrant in which power can be extracted from the solar cell. This near ohmic response indicates a very poor junction quality which is not able to effectively separate photogenerated carriers, with the solar cell instead acting largely as a resistor.

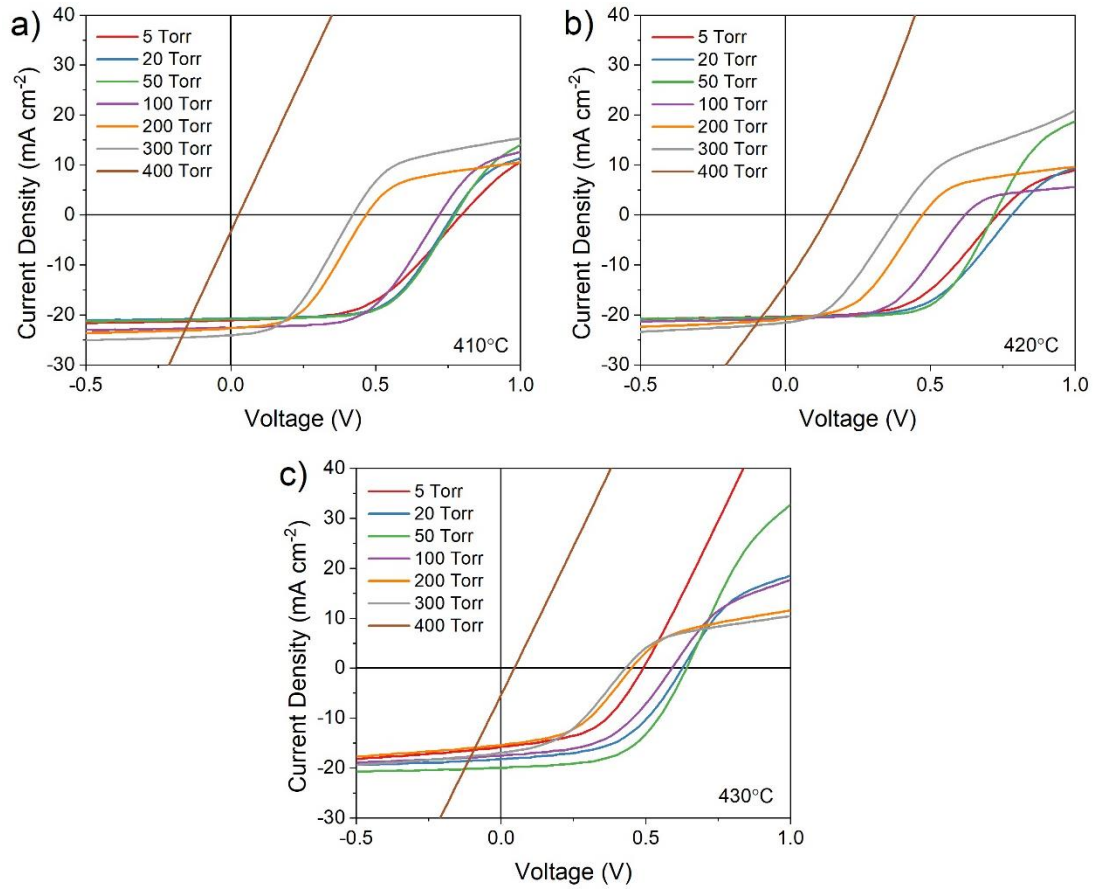

Figure 7.4: *JV* curves for the highest efficiency contact of CdTe/CdS devices grown under varied N_2 pressure and treated at (a) 410°C, (b) 420°C and (c) 430°C

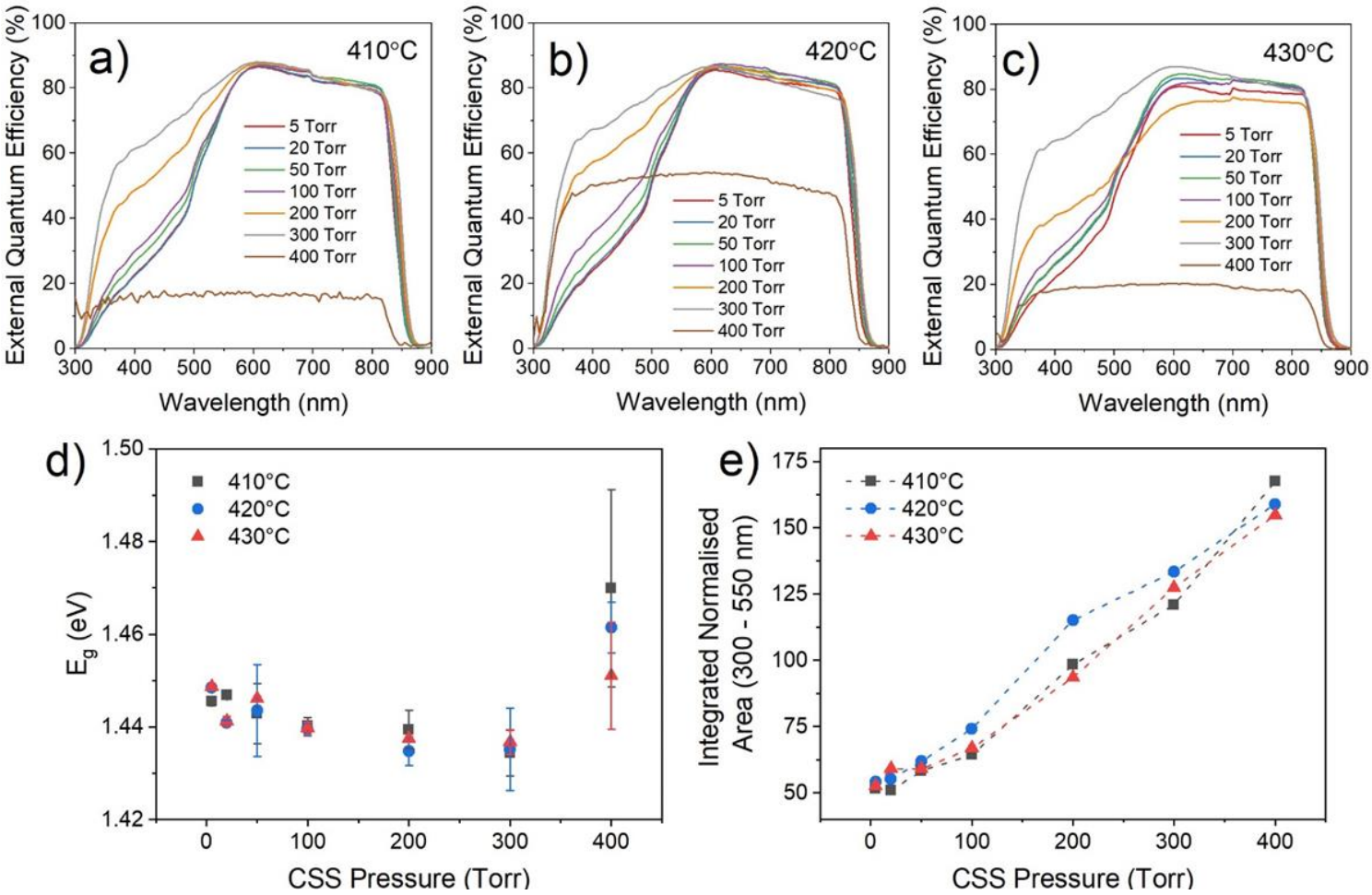

Figure 7.5: EQE spectra for devices grown on CdS under 5 – 400 Torr nitrogen and subject to $MgCl_2$ treatment at 410°C (a), 420°C (b) and 430°C (c). The minimum absorber band gap taken from linear extrapolation of the CdTe absorption edge (d) and integrated area of these EQE curves in the region of 300 – 550 nm after normalising to the point of maximum collection efficiency (e) are shown as a function of growth pressure

Figure 7.5(a-c) shows EQE curves for the highest efficiency contact from the CdS/CdTe devices described previously, grown under 5 – 400 Torr N_2 and $MgCl_2$ treated at temperatures between 410°C – 430°C. The minimum absorber band gap is determined from these EQE curves by extrapolating the linear section of the long wavelength cut-off region, and is plotted as a function of growth pressure for each activation temperature in Figure 7.5d. By normalising the EQE curves to the point of maximum collection efficiency and comparing the region 300 – 550 nm, an assessment of the blue response can be determined without influence of differences in overall collection efficiency. Figure 7.5e shows the area under these normalised EQE curves in the short wavelength region as a function of growth pressure. The effect of growth pressure and $MgCl_2$ treatment temperature on EQE curves will be discussed by considering the response at short, medium and long wavelength in turn:

a) Short wavelength region (300 – 550 nm)

This region is dominated by parasitic light absorption in the CdS layer, which absorbs light but does not contribute photocurrent since carriers are not collected efficiently. Therefore samples deposited at higher pressure, in which the thickness of the remaining CdS layer has been reduced by interdiffusion during long growth durations, show a comparatively higher EQE response in this region. The opposite applies for low deposition pressures whereby short growth durations lead to limited interdiffusion and therefore thicker CdS, resulting in a characteristic shoulder in the short wavelength EQE response. The shoulder region (~500-550 nm) therefore corresponds to the degree of interdiffusion between the CdS and CdTe layers. Devices grown at 400 Torr show a significantly reduced EQE response across all wavelengths due to a poor junction quality and therefore the efficiency is lower in the short wavelength region compared to other devices. However, there is no indication of parasitic CdS absorption, implying the CdS layer has been completely consumed by intermixing. Normalising the EQE curves allows the shape of the response to be compared directly instead of the absolute magnitude. By comparing the area under the normalised EQE curves in the short wavelength region, the effect of parasitic absorption in the CdS layer can be quantified since a CdS absorption shoulder will reduce the total area. This is shown in Figure 7.5e as a function of growth pressure for each $MgCl_2$ treatment temperature. The area under the short wavelength region of normalised EQE curves increases linearly with growth pressure, corresponding to a gradual increase in the extent of intermixing between the CdS and CdTe layers as the growth duration is increased. This does not vary with $MgCl_2$ treatment temperature, which confirms observations by Taylor et al [12] that CdS-CdTe intermixing for CSS grown devices occurs primarily during CdTe deposition rather than chlorine activation.

b) Mid wavelength region (550 – 850 nm)

This region corresponds to photons of energy between the band gap of CdS and CdTe. The maximum EQE response occurs around 600 nm, where photons have energy just below the CdS band gap and therefore are transmitted through to the photoactive CdTe layer. At higher wavelengths there is a small, gradual reduction in quantum efficiency due to longer wavelength photons penetrating deeper into the CdTe layer, meaning photogenerated carriers are produced further from the junction at which they are separated. For each activation temperature, all devices show a similar response with no systematic change with growth pressure. However, devices which are grown at the same pressure but undergo $MgCl_2$ treatment at different temperatures show subtle differences. Higher $MgCl_2$ temperature is correlated with a flatter gradient indicating better collection further into the device. This is likely due to the increased depletion width for high activation temperatures as a result of lower doping density, as shown in Figure 7.6e.

c) Long wavelength region (850 – 900 nm)

The long wavelength cut-off of the EQE curves is determined by the minimum band gap of the absorber layer, which comprises of an intermixed CdS_yTe_{1-y} phase for these devices and is therefore expected to vary between samples according to on the degree of interdiffusion. Figure 7.5d shows that the minimum absorber band gap decreases with increasing growth pressures up to 300 Torr, irrespective of $MgCl_2$ treatment temperature. This is consistent with the extended growth durations which accompany higher pressure growth resulting in more interdiffusion of the CdS and CdTe layers, with dilute sulphur compositions reducing the band gap of CdS_yTe_{1-y} compared to CdTe via the bowing effect [24]. At 400 Torr, there is a reversal of this trend whereby the absorber band gap increases. As interdiffusion continues and the phase becomes more sulphur rich, the band gap of CdS_yTe_{1-y} increases towards that of CdS. The lack of a dependence on activation temperature again confirms that interdiffusion occurs primarily during deposition [12].

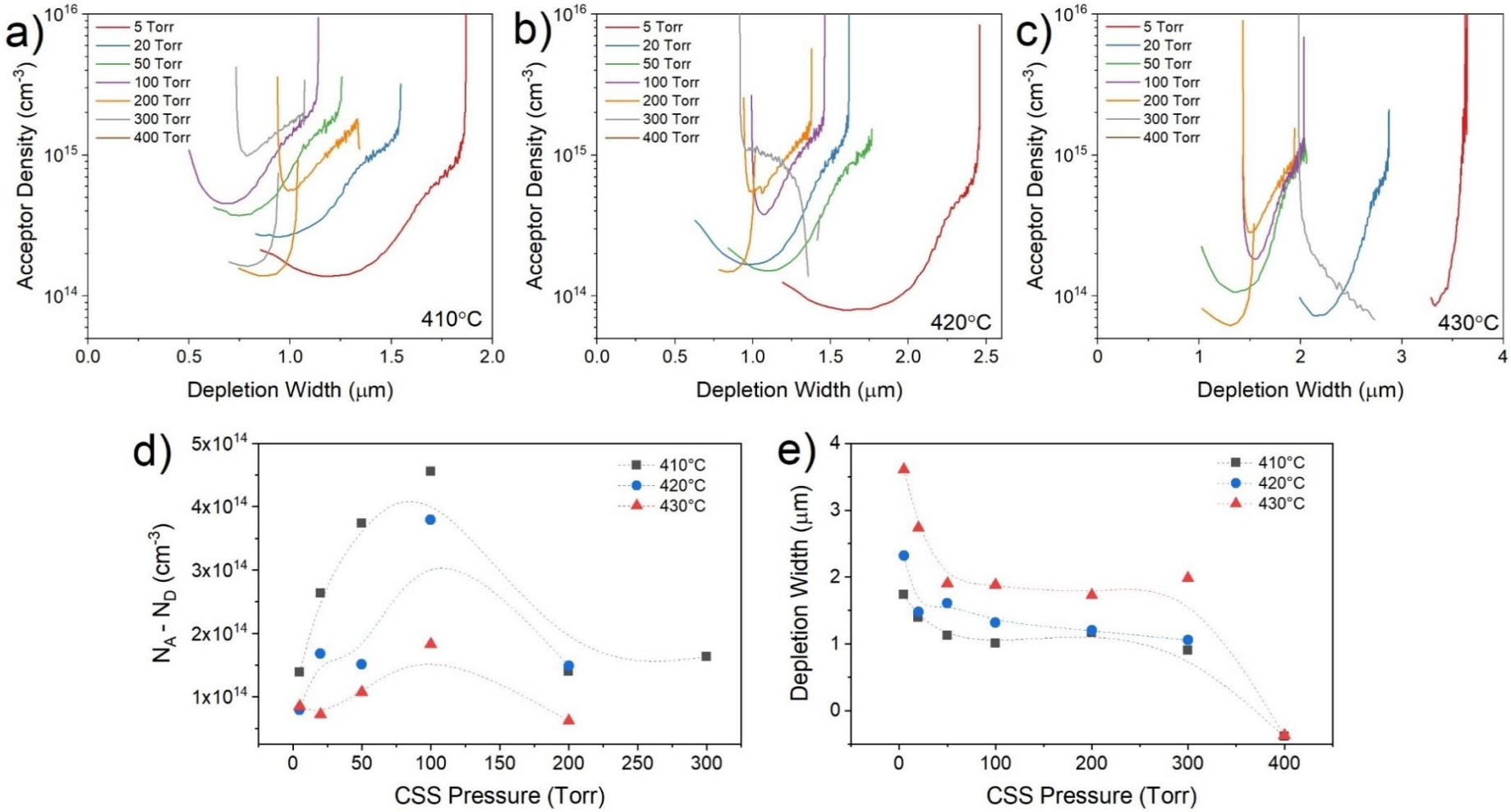

Figure 7.6: Acceptor density profiles for CdTe/CdS solar cells grown under 5 – 400 Torr nitrogen and $MgCl_2$ treated at 410°C (a), 420°C (b) and 430°C (c), with the acceptor density estimated from the minima of each curve shown as a function of pressure (d) and depletion width at zero bias shown in (e)

Figure 7.6(a-c) shows acceptor density profiles determined from Mott-Schottky analysis of *CV* measurements for the same set of devices. The net doping density is estimated from the minima of each of these curves and is shown as a function of growth pressure in Figure 7.6d for each treatment temperature, as well as the depletion width at zero applied bias shown in Figure 7.6e. All devices grown at 5 Torr show a similar net doping density of ~1×10^{14} cm^{-3} for each treatment temperature. This increases with growth pressure before peaking at 100 Torr for each treatment temperature, with a maximum doping density of 4.5×10^{14} cm^{-3} obtained for devices treated at 410°C. As the doping density increases with higher pressure, the depletion width decreases accordingly to maintain charge neutrality. After a rapid decrease in the depletion width for growth pressures up to 100 Torr, this plateaus for 200 Torr and 300 Torr devices, whilst devices grown at 400 Torr showed a negative depletion width implying the devices are not of sufficient quality to allow accurate analysis. There is a clear dependence on the activation temperature for these devices, with higher temperature chlorine treatments resulting in lower doping density and larger depletion width. This can explain to some extent the deterioration in performance for increased $MgCl_2$ temperatures. Low doping density will itself limit efficiency, and the progressive decrease could indicate carrier compensation which will introduce defect states and aid recombination.

The acceptor density profiles for devices grown above 100 Torr show atypical behaviour. This includes profiles without a clear minimum which makes estimating the net bulk doping density challenging, double peaks which result from a contribution from the back-contact, and unphysical negative depletion widths. These results should be interpreted cautiously, since the *CV* analysis undertaken here relies on several assumptions such as a uniformly doped, one sided junction. These assumptions are likely to become progressively less valid with the longer growth times necessary for high pressure deposition, as the window layer is consumed during interdiffusion of CdS and CdTe.

In any case, the lack of intentional extrinsic doping limits acceptor concentration to the mid 10^{14} cm^{-3} range for all devices shown here, regardless of processing conditions. There are several reasons why growth pressure, and by extension growth duration (Table 7.2), could affect doping density, including out-diffusion of electrically active impurities from the glass substrate such as sodium or potassium, grain size affecting the movement of dopants, and chlorine availability during the activation treatment.

7.2.5 Summary of findings for CdS/CdTe solar cells

The effect of deposition pressure and $MgCl_2$ treatment temperature on the performance of CdS/CdTe solar cells has been investigated here to determine the optimal processing conditions and to explore the limitations of this device structure. Increased growth pressure was shown to result in CdTe films with a larger, more randomly oriented grain structure which is consistent with previous observations [25]. However, increased CdTe grain size did not translate to improved device performance. Instead, higher pressure growth is accompanied by longer deposition times which results in excessive intermixing of the CdS and CdTe layers as well as larger grains. This demonstrates the difficulty in isolating the influence of a single processing variable such as growth pressure on device performance, since there can be several interrelated effects on nucleation conditions, grain structure, junction intermixing and the distribution of impurities.

Similarly, increasing the $MgCl_2$ activation temperature above 410°C causes a rapid decrease in device efficiency despite no further intermixing of the CdS and CdTe layers. Instead, these overtreated devices have a lower doping density which could indicate a more compensated defect structure. These results show that the CdS/CdTe architecture is clearly limited in terms of the thermal budget available for both growth of the CdTe layer and chlorine treatment of the device. However, it is not clear whether this limitation is intrinsic to devices with a CdTe based absorber layer, or whether other device structures might tolerate higher deposition and treatment temperatures which may offer a route to improved performance. This is investigated further in sections 7.3 and 7.4.

7.3 CdTe solar cells with a SnO_2 window layer

7.3.1 Introduction

In the previous section, high temperature growth of CdTe films onto CdS substrates was shown to result in the intermixing and in severe cases consumption of the CdS window layer, limiting the thermal budget available during the processing of this device structure. Furthermore, the $MgCl_2$ activation temperature was limited to 410°C to prevent overtreatment which reduced the net acceptor density and results in lower efficiency. In comparison, section 6.4 demonstrated that a CdTe/SnO_2 device architecture was more tolerant to an aggressive NaF and $MgCl_2$ treatment than the more typical CdTe/CdS structure. With this in mind, in this section CdTe films are grown directly onto SnO_2 coated substrates to explore any potential new parameter space offered by the more robust window layer.

7.3.2 Device fabrication

Devices were deposited on TEC15M substrates which are identical to the TEC15 substrates used previously, but also include a 100 nm undoped SnO_2 layer deposited by the manufacturer via chemical vapour deposition. This replaced the CdS window layer and therefore these substrates were loaded directly into the CSS chamber following cleaning. CdTe films were then grown under nitrogen pressures between 5 – 400 Torr, varying the growth time to achieve 7 μm thickness for each sample (Table 7.2). These films were then processed into devices by undergoing $MgCl_2$ treatment at temperatures between 410 – 430°C, followed by etching and metallisation in the same way as previously described in section 7.2.2.

7.3.3 Structural analysis of CdTe films deposited on SnO_2 at varied pressure

Figure 7.7(a – g) shows SEM images of the back surface of as deposited CdTe films grown directly onto SnO_2 coated glass substrates at pressures between 5 – 400 Torr. Histograms of grain size are also shown for each sample. The average grain size was determined by manually tracing grain boundaries and measuring the area of >200 grains per sample using ImageJ software. The grain size was then calculated as the radius of a circle with equivalent area, and the average grain radius is shown as a function of growth pressure in Figure 7.7h.

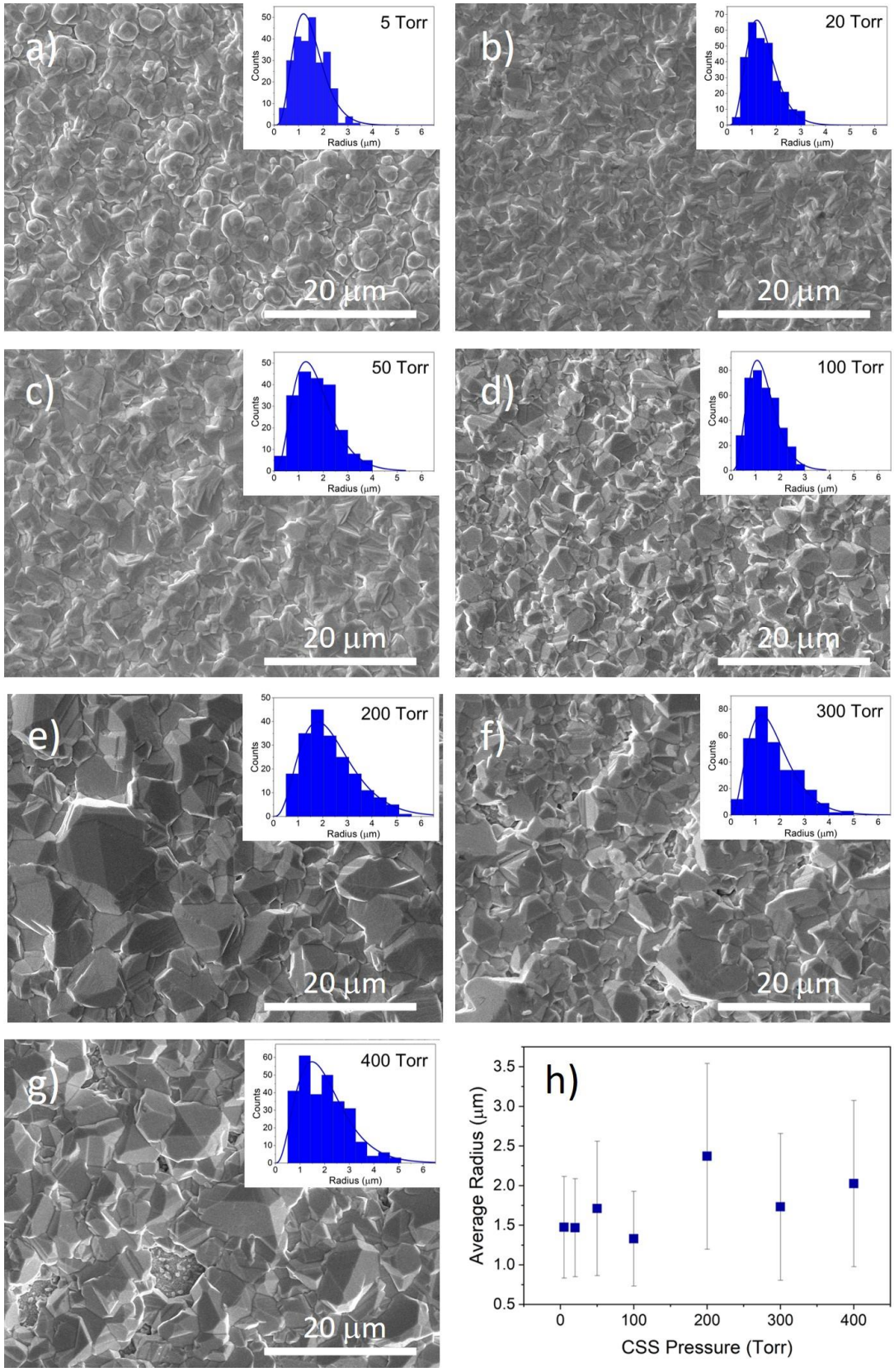

Figure 7.7: SEM images of the back surface of as grown CdTe films deposited on SnO_2 at pressures between 5 – 400 Torr (a) – (g) with the grain size distribution shown inset, as well as the mean radius plotted as a function of deposition pressure (h)

The CdTe films grown at 5 Torr (Figure 1.7a) shows a rounded grain structure with less pronounced hexagonal facets than previously observed for growth on CdS substrates (Figure 1.1a), which is consistent with a reduction in [111] orientation evidenced from XRD measurements in Figure 1.8. Previous reports have shown that the CdS layer plays an important role in templating the [111] oriented growth of the CdTe [25], and therefore its replacement with SnO_2 is expected result in more randomly nucleated islands. Grains become less rounded and more irregularly shaped as the growth pressure is increased to 20 Torr and 50 Torr, and well-defined crystal facets become clearer for growth pressures above 100 Torr.

Whilst higher pressure growth leads to a visibly larger grain structure, this is not obvious from the average grain size shown in Figure 7.7h, which is heavily scattered. Instead the maximum grain size increases with growth pressure which results in more skewed histograms, but the average remains low due to the presence of many smaller grains. It is noted that there are large uncertainties associated in the average grain size taken from measurement of manually defined grains where grain boundaries are not clearly distinguished, and a technique such as EBSD would allow for a much more accurate assessment. However, it is clear from these results that dependence of grain size of growth pressure is much weaker for CdTe films grown on SnO_2 substrates compared to the CdS substrates shown in Figure 7.1.

Whereas low growth pressures result in a compact, continuous CdTe film, high growth pressures (Figure 7.7f and Figure 7.7g) result in large areas of exposed SnO_2 substrate which was not observed when deposited onto CdS. This is exacerbated by high pressure growth, and can be observed on a wider scale using backlit optical microscopy shown in in Figure 7.8(a-c). Here, the sample is illuminated from behind the device and therefore bright areas correspond to regions of poor CdTe coverage, resulting in pinholes and therefore direct contact between the SnO_2 and Au in a device. No pinholes were observed by optical microscopy for growth pressures up to 100 Torr, however the pinhole density is seen to increase rapidly above 200 Torr. To quantify the pinhole area, the as grown films were illuminated with above band gap light between 500 - 800 nm, which should be almost entirely absorbed by the ~7 μm thick CdTe layer. In this way the fractional pinhole area could be estimated by the average light transmission, which is given in Figure 7.8d and gradually increases with higher deposition temperatures.

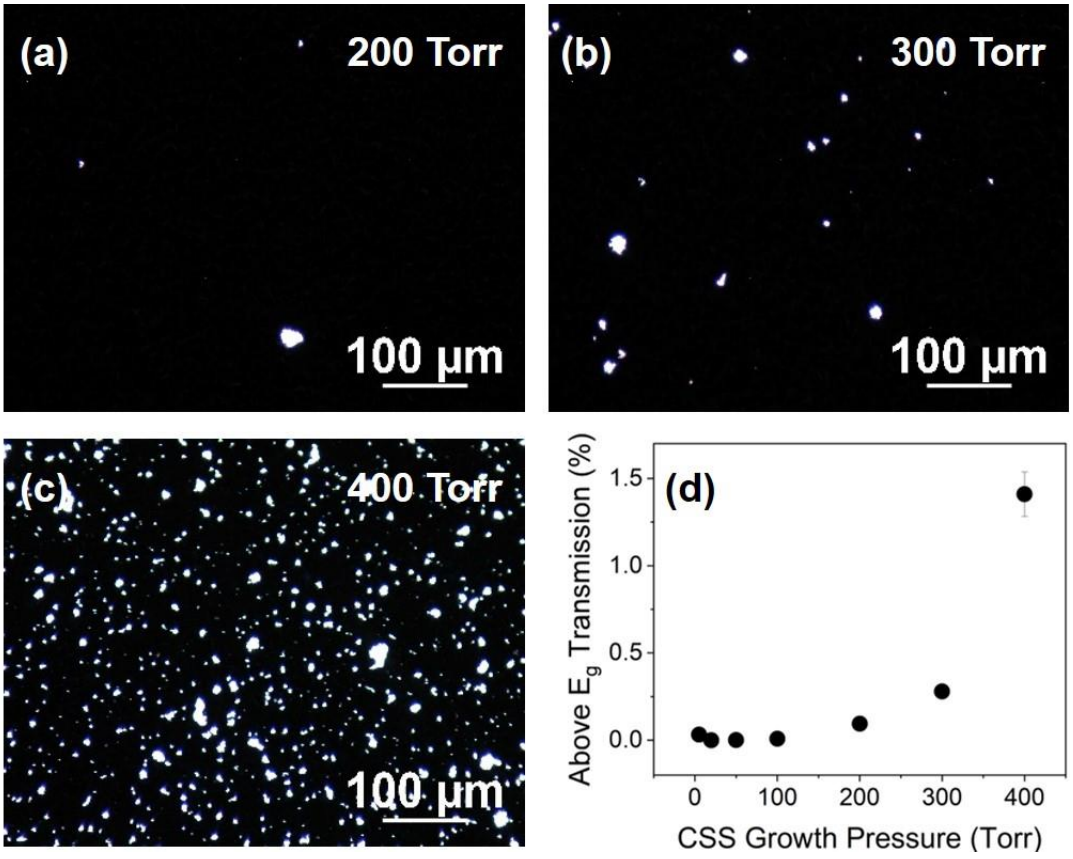

Figure 7.8: Backlit optical microscope images showing the pinhole density for SnO_2/CdTe films grown at (a) 200 Torr, (b) 300 Torr, (c) 400 Torr and (d) the percentage of above band gap light transmitted through samples of CdTe on SnO_2 substrates prior to $MgCl_2$ treatment

The absence of hexagonal crystal facets and lack of systematic grain size change with growth pressure shown in SEM images, as well as areas of exposed substrate shown from optical microscopy suggests growth of CdTe is substantially different on SnO_2 in comparisons to CdS. It can also be seen that SnO_2 is an especially poor choice of substrate for high pressure growth. The SnO_2 layer, which is deposited via CVD from the manufacturer, is likely to be rougher than the sputtered CdS layer which may smooth out the underlying roughness of the substrate. This increased roughness could therefore alter the nucleation and growth of CdTe. Alternatively, differences in the lattice contact, bonding environment, and crystal structure of SnO_2 substrates compared to CdS could contribute to the observed differences in the growth of CdTe films and the resulting grain structure.

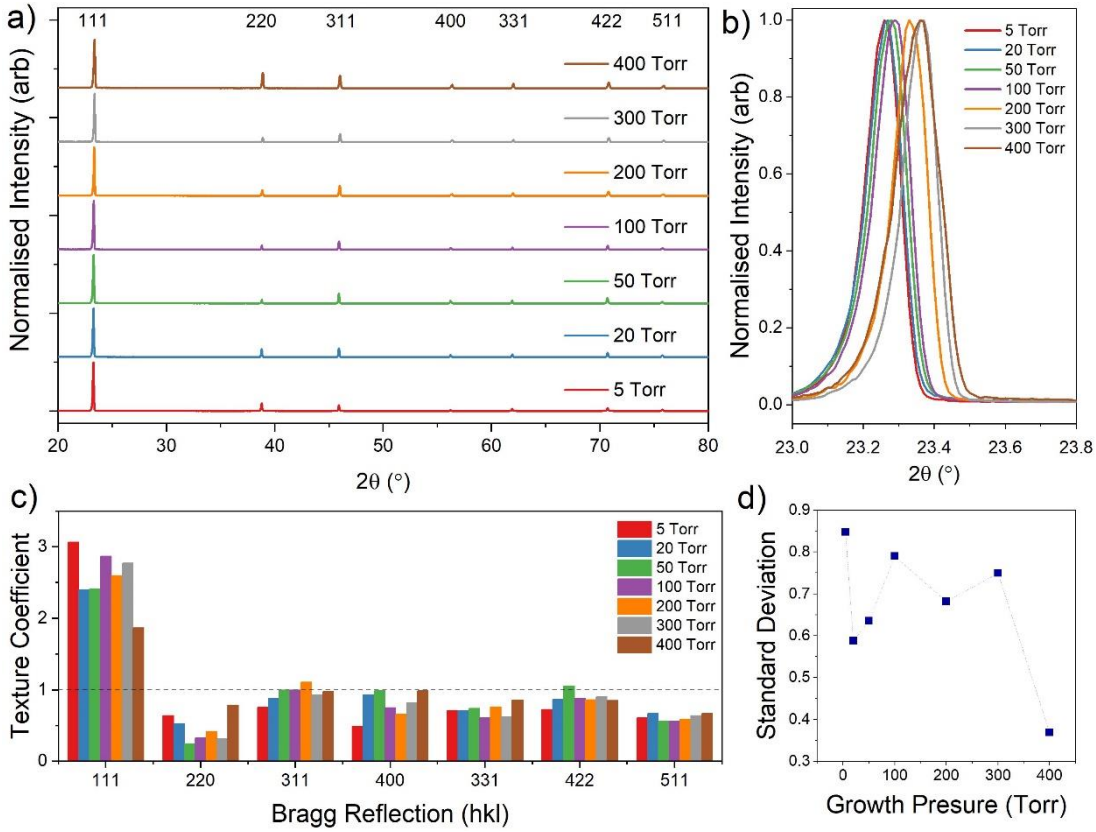

Figure 7.9: XRD data for 7 μm CdTe films grown on SnO_2 coated substrates under varying pressure of nitrogen (a), with higher magnification of the 111 peak shown in (b). The texture coefficient for each Bragg reflection at each growth pressure is given in (c) as well as the standard deviation of the texture coefficient for each sample in (d)

Figure 7.9 shows XRD data for the as grown CdTe films deposited on SnO_2, under varying nitrogen pressure, whereby increased pressure results in longer growth times to maintain constant thickness (Table 7.2). The normalised diffraction patterns in Figure 7.9a show that the to the 111 peak is dominant for all samples, which is shown at higher magnification in Figure 7.9b. There is no variation in peak shape in contrast to films deposited on CdS (section 7.2.3), however there is a pronounced change in peak position. This gradual peak shift indicates that the lattice constant (a_0) decreases linearly from 6.62 Å to 6.59 Å as deposition pressure increases from 5 Torr to 300 Torr, with no further change for the 400 Torr sample. In comparison, the expected lattice constant for a powdered (unstrained) CdTe sample is 6.48 Å [26], which is significantly smaller than calculated for all samples here. The larger lattice constant for these films than both a powdered sample and those grown on CdS suggest there is more strain present in these films, which could be a result of growth on a highly lattice mismatched substrate [27]. Whereas interdiffusion of CdS and CdTe is typically relied on to relax the 10% lattice mismatch in CdS/CdTe devices [28], the absence of a CdS layer in these samples means the strain is retained despite the prolonged high temperature growth. The decrease of lattice constant with growth duration could be due to some degree of intermixing

at the interface, although this is expected to be minimal [29] and not extend throughout the full device. This significant change in lattice constant indicated by back surface measurements of ~7 μm thick CdTe films suggest the variation in growth conditions is having an impact on the bulk CdTe film beyond what might be expected for tin and/or oxygen incorporation from the substrate decreasing the average lattice constant. This could be an effect of the longer growth times for higher pressure depositions causing film relaxation at the interface, which is consistent with a gradual decrease in lattice constant towards the unstrained bulk value

Figure 7.9c - d show that the randomisation of texture with growth time that is observed on CdS substrates is not observed for SnO_2. All films display a [111] preferred orientation. However, this does not change systematically with growth duration, and no trend observed as a function of nitrogen pressure in either the texture coefficients or their standard deviation is observed. CdS is reported to template the growth of CdTe in the [111] direction [30] and therefore the use of SnO_2 as a substrate will result in fewer [111] oriented islands during the nucleation stage of CdTe deposition. This can be seen by comparing the diffraction patterns of CdTe grown at 5 Torr on CdS and SnO_2 substrates whereby low pressure growth on CdS results in almost exclusive [111] orientation with very small signals from the other reflections (Figure 7.1). In contrast Figure 7.9 shows that whilst CdTe grown on SnO_2 substrates retains a [111] preferential orientation, there are also relatively strong signals corresponding to reflections from several orientations even for films deposited at 5 Torr. SnO_2 clearly has an impact on the nucleation and subsequent growth of CdTe films and, which could result from the roughness, chemical composition, and crystal structure of the substrate. This means that a preferred [111] orientation for CdTe films that is insensitive to growth pressure, which contrasts with CdS substrates where the texture can be more effectively controlled with growth pressure.

7.3.4 Device analysis of CdTe/SnO_2 solar cells deposited at varied pressure

The films described above were then processed into solar cells comparing $MgCl_2$ activation treatments at 410°C, 420°C and 430°C for each growth pressure. The performance parameters for these devices are shown in Figure 7.11, with the *JV* curves for the highest efficiency contact of each device shown in Figure 7.10. This shows that $MgCl_2$ treatments at 410°C produce very low efficiency devices regardless of growth pressure. Although there is an initial improvement in all performance parameters with increased pressure up to 100 Torr, beyond this the open circuit voltage is decreased, limiting the maximum efficiency to 1.6% for the 410°C series. These devices are primarily limited by low fill factor which can be seen in Figure 7.10a to result from an 'S' shaped *JV* curve. This is commonly seen for CdTe junctions with

MZO [4,7], and typically attributed to poor conduction band alignment which limits electron extraction from the CdTe layer. Increasing the treatment temperature to 420°C improves device efficiency due to an increased short circuit current density and fill factor.

Figure 7.10b shows a better diode response with intermittent and much less severe 'S' shaped curves resulting in a dramatic reduction in series resistance and increased shunt resistance. There is a further increase in efficiency for devices treated at 430°C due to increased fill factor caused by decreased series resistance. Further tests on higher temperature $MgCl_2$ treatments indicate that there is no additional improvement above 430°C, whereby devices become overtreated.

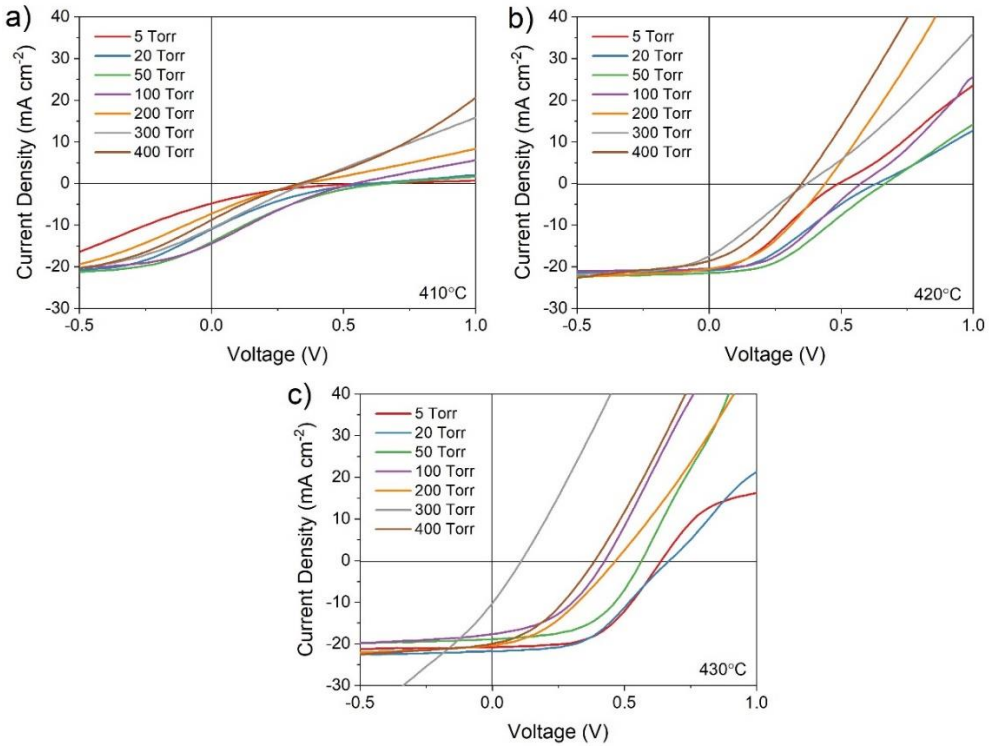

Figure 7.10: *JV* curves for the highest efficiency contact of CdTe/SnO_2 devices grown under varied N_2 pressure and treated at 410°C (a), 420°C (b) and 430°C (c)

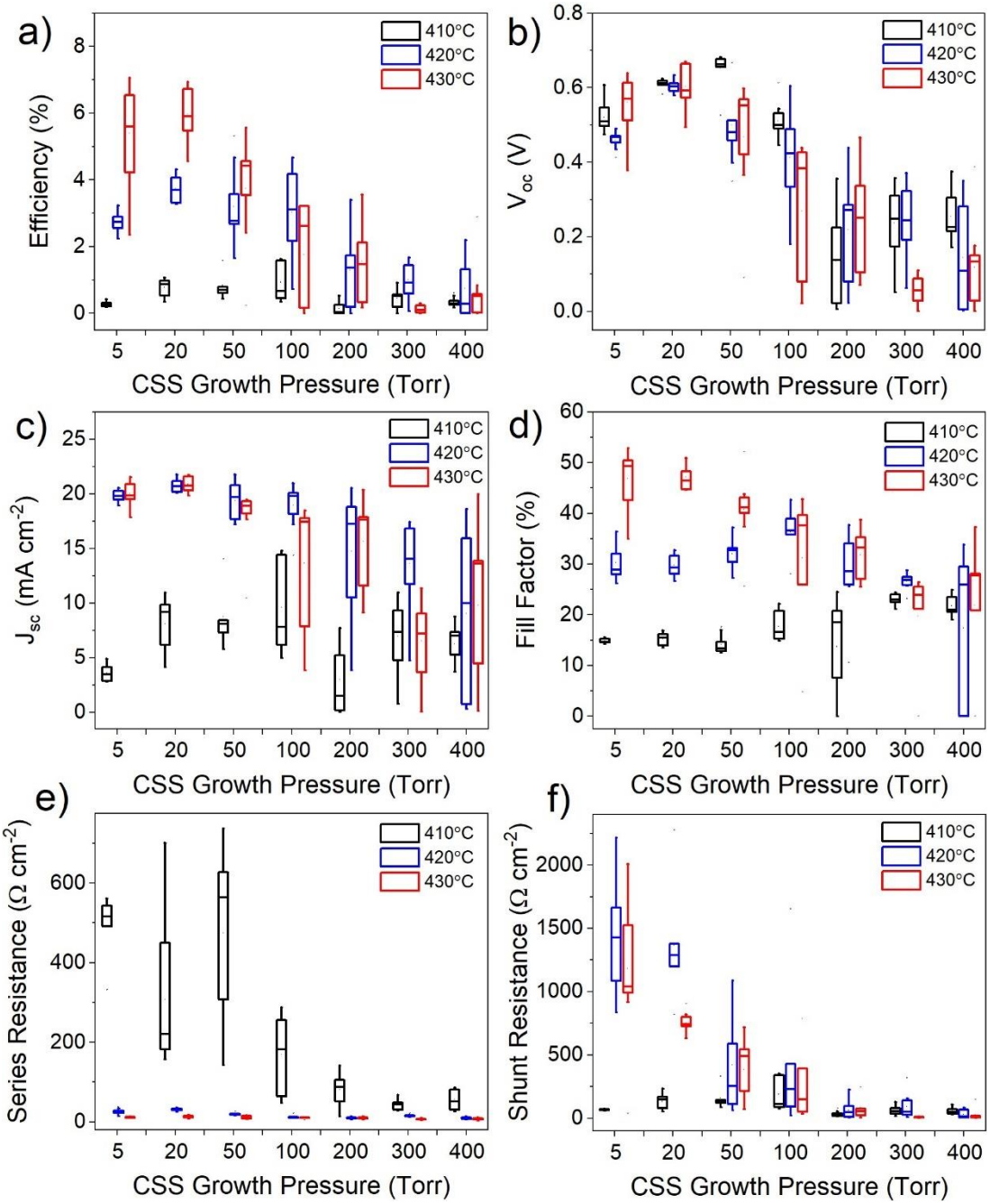

Figure 7.11: Box and whisker plots showing *JV* performance parameters for SnO_2/CdTe devices grown under 5 - 400 Torr of nitrogen, activated at 410°C, 420°C, 430°C. The box boundaries show the upper and lower quartiles with a horizontal line for the median value, and the range given is by the whiskers. The efficiency (a), open circuit voltage (b), short circuit current density (c), fill factor (d), series resistance (e) and shunt resistance (f) is given as a function of growth pressure

For all $MgCl_2$ treatment temperatures, peak device efficiency is achieved at growth pressures below 100 Torr. Therefore, despite indications a less strained CdTe layer (Figure 7.9) with slightly increased grain size (Figure 7.7) for high pressure growth, this has not translated to improved efficiency. Whilst series resistance does decrease for higher pressure growth, this is offset by a rapid deterioration in shunt resistance and V_{oc} which leads to a decrease in

efficiency. This reduced shunt resistance can be explained by incomplete coverage of CdTe on the SnO_2 substrate shown in Figure 7.8, causing an increase in the fractional area of pinholes which is visible by eye. This confirms that CdTe growth is strongly influenced by the SnO_2 substrate, leading to incomplete substrate coverage at high pressures resulting in a high density of pinholes which are not observed for growth on CdS.

The 'S' shaped curves observed for low treatment temperatures are common for CdTe devices and typically attributed to a spike in the conduction band at the interface between the absorber and window layer as a result of a small electron affinity. Examples of spike, flat and cliff type conduction band alignments, simulated using SCAPS, are shown in Figure 7.12(a-c) to demonstrate the importance electron affinity has in producing a favourable band alignment. Whilst a small (ΔE_C < 0.1 eV) spike in the conduction band can be beneficial by reducing recombination at the interface, a large spike would result in a current blocking effect which manifests as an 'S' shape in *JV* curves such as those seen in Figure 7.10
Figure 7.10. This phenomenon is observed in a wide range of solar cell technologies [31] and is more generally attributed to the presence of a charge transport barrier. The reported electron affinity of around 4.5 eV for bulk SnO_2 matches well with that of CdTe and therefore a flat band alignment would be expected [32]. However, this is likely to be an overly simplistic approach. Predicting the band alignment at a heterojunction interface from literature values of bulk materials is challenging [33], and is further influenced by the location of the Fermi level within both the window and absorber layers and defects near the interface. An example of the effect of interfacial defects is shown in Figure 7.12(d-f) whereby increasing the defect density causes pinning of the Fermi level near the mid gap. This forces upward band bending at the interface which acts as a barrier to electrons flowing towards the window layer. This would be expected to have a qualitatively similar impact on *JV* curves as a spike in the conduction band, with a secondary charge transport barrier in both cases causing an 'S' shaped curve.
It is unclear exactly how the $MgCl_2$ treatment affects the band alignment of the CdTe/SnO_2 junction, since this is determined by multiple factors including the relative band positions, doping density of each material and defects that results in Fermi level pinning [1]. The reported work function of SnO_2 varies significantly in literature and shows strong sensitivity to processing conditions [34]. This is further complicated by surface dipole effects which make accurate measurement of the work function challenging and means bulk literature values are not likely to accurately represent the conditions a real interface [35,36]. However, removal of the 'S' shaped *JV* curves upon high temperature $MgCl_2$ treatment suggests that the band alignment reduces is improved by removal of a charge transport barrier at the junction interface, resulting in a flatter conduction band alignment. The $MgCl_2$ treatment is unlikely to have a substantial impact on the electron affinity of either layer, and *CV* measurements do not indicate significant

variation in CdTe doping density for different treatment temperatures (Figure 7.14e). This leaves either a change in the work function of the SnO_2 layer, or passivation of interfacial defects that cause a secondary barrier as the likely sources of the improvement [37].

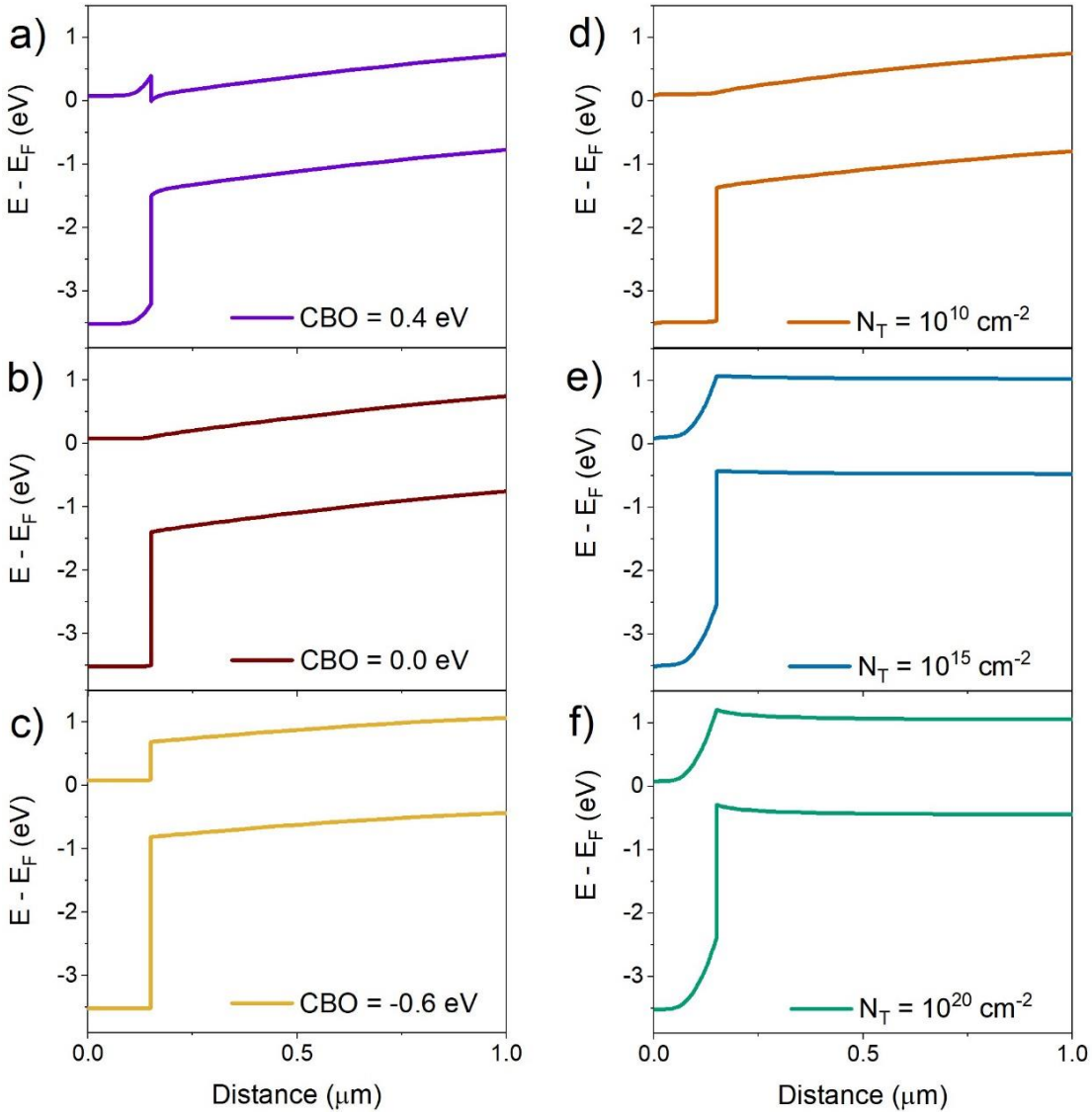

Figure 7.12: Examples of equilibrium band diagrams *p-n* heterojunctions showing the effect of a conduction band offset (a-c) and interfacial defect density (d-f), simulated using SCAPS. The conduction band offset (CBO) is varied to produce a spike (a), flat (b) and cliff (c) type conduction band alignment, assuming a defect-free interface. Band alignments where interfacial defect density (N_T) is (d) 10^{10} cm^{-2}, (e) 10^{15} cm^{-2} and (f) 10^{20} cm^{-2} are also shown

Figure 7.13(a-c) shows the normalised EQE spectra for the highest efficiency cell from each device, corresponding to the *JV* curves shown in Figure 7.10

Figure 7.10. The band gap of $MgCl_2$ treated samples is taken from the long wavelength EQE cutoff and shown as a function of growth pressure in Figure 7.13d. The band gap of the untreated CdTe films before processing into solar cells is also shown at each pressure for comparison, determined from UV-vis measurements via the Tauc method. Figure 7.13e shows the discrepancy between the J_{sc} for each sample determined directly from *JV* measurements and calculated from EQE curves of the same cells.

There is a square EQE shape for all measured cells indicating high collection efficiency across all wavelengths owing to of the wide band gap of SnO_2 in comparison to CdS. There is noticeable variation in long wavelength collection (700 – 850 nm) that is most apparent for 410°C and 430°C series, however no systematic trend could be identified in either case which might infer a strong sensitivity to small variations in carrier lifetime for these devices. The minimum absorber band gap was taken from the intercept of the CdTe absorption onset with the *x*-axis for each treatment temperature and is plotted as a function of growth pressure in Figure 7.13d, which also shows the band gap of untreated films. This shows that the CdTe band gap is not affected by the $MgCl_2$ treatment temperature, and therefore confirms that any improvement in band alignment inferred from Figure 7.10 is not due to changes in band structure on the absorber side. There is a small increase in band gap with increased growth pressure, although this is a minor effect with a maximum variation of 0.016 eV between all measured devices. This might be caused by some small degree of intermixing at the interface, since SnO_2 substrates have reportedly aided oxidation of overlayers during CdTe processing [29]. Alternatively, variation in the amount of strain at the interface could alter the absorber band gap, and is expected to show a dependence on growth pressure according to XRD measurements (Figure 7.9). The band gap of as grown films, which were not processed into full devices, shows a much clearer trend compared to the $MgCl_2$ treated film, with maximum band gap at 50 Torr before decreasing linearly with growth pressure. This trend is subtly different than for the films that were processed into devices, and it remains unclear whether this is due to the difference in the method of measuring band gap or changes that occur upon $MgCl_2$ treatment.

Figure 7.13e shows the difference between the short circuit current density of devices measured directly from *JV* curves compared to integrating the EQE curves and accounting for the AM1.5G solar spectrum. In theory both values should be identical, however the data above shows EQE measured J_{sc} values are consistently higher than from *JV* measurements. This difference can be explained by the different operating conditions under which the cells are measured, with EQE spectra collected in the dark and perturbed only by a small AC

monochromatic light signal whereas *JV* measurements are taken under AM1.5G light. Therefore, low injection conditions measured by EQE do not represent typical operating conditions for a solar cell, and so *JV* measurements are considered to give a more accurate estimate of J_{sc}. Nonetheless, the difference between these two measured values can give insight into the way in which photogenerated carriers can modify junction transport. Low short circuit current compared to integrated EQE can indicate a barrier to photocurrent whereby small current densities such as those observed during EQE measurements can pass such a barrier via thermionic emission, but high current densities observed under AM1.5G illumination cannot [37]. Therefore the difference between J_{sc} determined by *JV* and EQE measurements can give a rough indication of the size of the barrier. In this way, Figure 7.13e would indicate $MgCl_2$ treatment at 410°C produces a large barrier for photogenerated carriers, which is alleviated to some extent by higher growth pressure. This is likely due to the long growth duration acting as an in-situ anneal step.

The J_{sc} difference for 420°C and 430°C $MgCl_2$ treatments is further reduced, although does not vary with treatment temperature or growth pressure which suggests the barrier height is lowered as much as possible. This interpretation would be consistent with the findings from Figure 7.10 whereby the 'S' shaped *JV* curves result from misaligned conduction bands at the interface between SnO_2 and CdTe. The exact nature of the band alignment at the interface which causes this barrier, as well as the mechanism by which it is alleviated by higher temperature $MgCl_2$ treatment, remains unclear. However, given the improvement with growth pressure inferred from Figure 7.13e for the 410°C series, which is consistent with indications of reduced strain in as grown films (Figure 7.9), a lower interfacial defect density for high growth pressure or high temperature $MgCl_2$ treatment offers a plausible explanation.

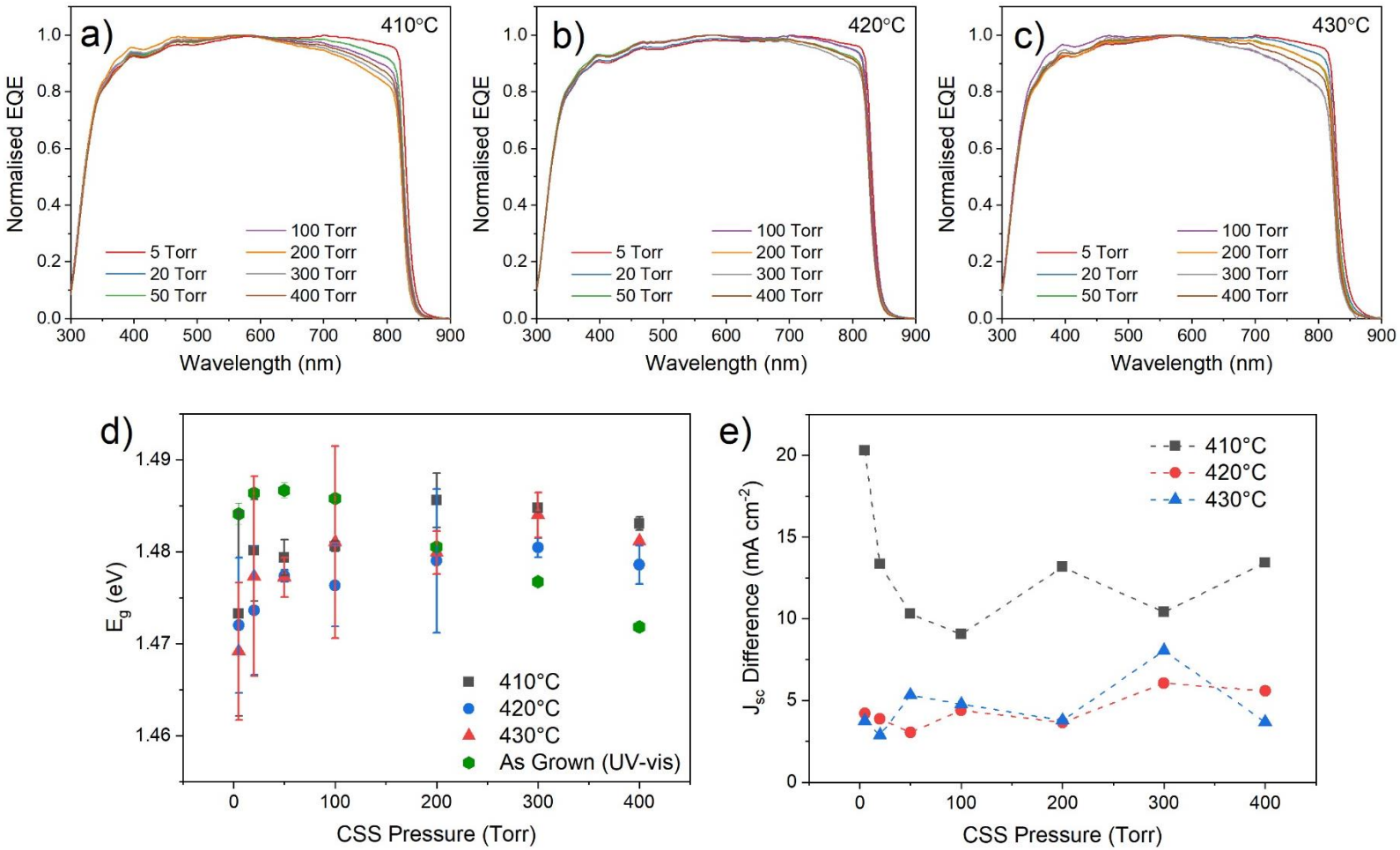

Figure 7.13: Normalised EQE spectra for devices grown on SnO_2 under 5 – 400 Torr nitrogen and subject to $MgCl_2$ treatment at 410°C (a), 420°C (b) and 430°C (c) as well at the minimum absorber band gap taken from the intercept at long wavelength compared to the band gap of as grown films estimated from absorption data using the Tauc method (d) and the difference between short circuit current density measured from *JV* curves and integrated EQE curves (e)

Figure 7.14 shows the results of *CV* measurements of the highest performing contact from each of the devices described previously. Figure 7.14(a-c) shows acceptor density vs depletion width curves for each growth pressure and $MgCl_2$ treatment temperature. Figure 7.14d shows the bulk acceptor density estimated from each curve minima, and the depletion width at zero bias given as a function of growth pressure is given in Figure 7.14e. For each treatment temperature the acceptor density increases by an order of magnitude at growth pressures above 5 Torr, reaching ~10^{15} cm^{-3} for all devices except for an outlying device in the 430°C series which was poorly rectifying as shown in Figure 7.10c. This is roughly a factor of two more than the highest acceptor densities measured on CdS in Figure 7.6 which might indicate that the SnO_2/CdTe architecture is more amenable to *p*-type doping due to a simpler defect structure in the absence of sulphur diffusion.

Since no dopants are intentionally added into the devices, it is unclear what is causing the increase in acceptor concentration. It is generally thought that intrinsic doping via tellurium rich growth is insufficient to obtain high doping densities [38]. Therefore, any compositional change that might occur with varied growth pressure is unlikely to be directly responsible for the change in doping density, although may have an impact on the incorporation of extrinsic dopants. Prolonged exposure to elevated temperatures during CdTe deposition for high pressure growth will result in out-diffusion of impurities from the underlying substrate, which may act as *p*-type dopants. Sodium is the most likely contaminant and is already present at concentrations above 10^{17} cm^{-3} in the source material, making it readily available. If this is the active dopant, this would imply an activation ratio of ~1% which would indicate that strong compensation effects require lots of excess sodium to achieve high levels of *p*-type doping.

Although varying the $MgCl_2$ treatment temperature leads to significant differences in device performance, the doping density and depletion width are unaffected. This lack of correlation indicates that efficiency is not primarily limited by doping density in the CdTe layer, but instead by a small built in voltage due to poorly optimised band alignment. This will contribute to the smaller space charge region for observed for devices in Figure 7.14e compared to CdS/CdTe devices described in Figure 7.6e, although this will also be influenced by higher doping density.

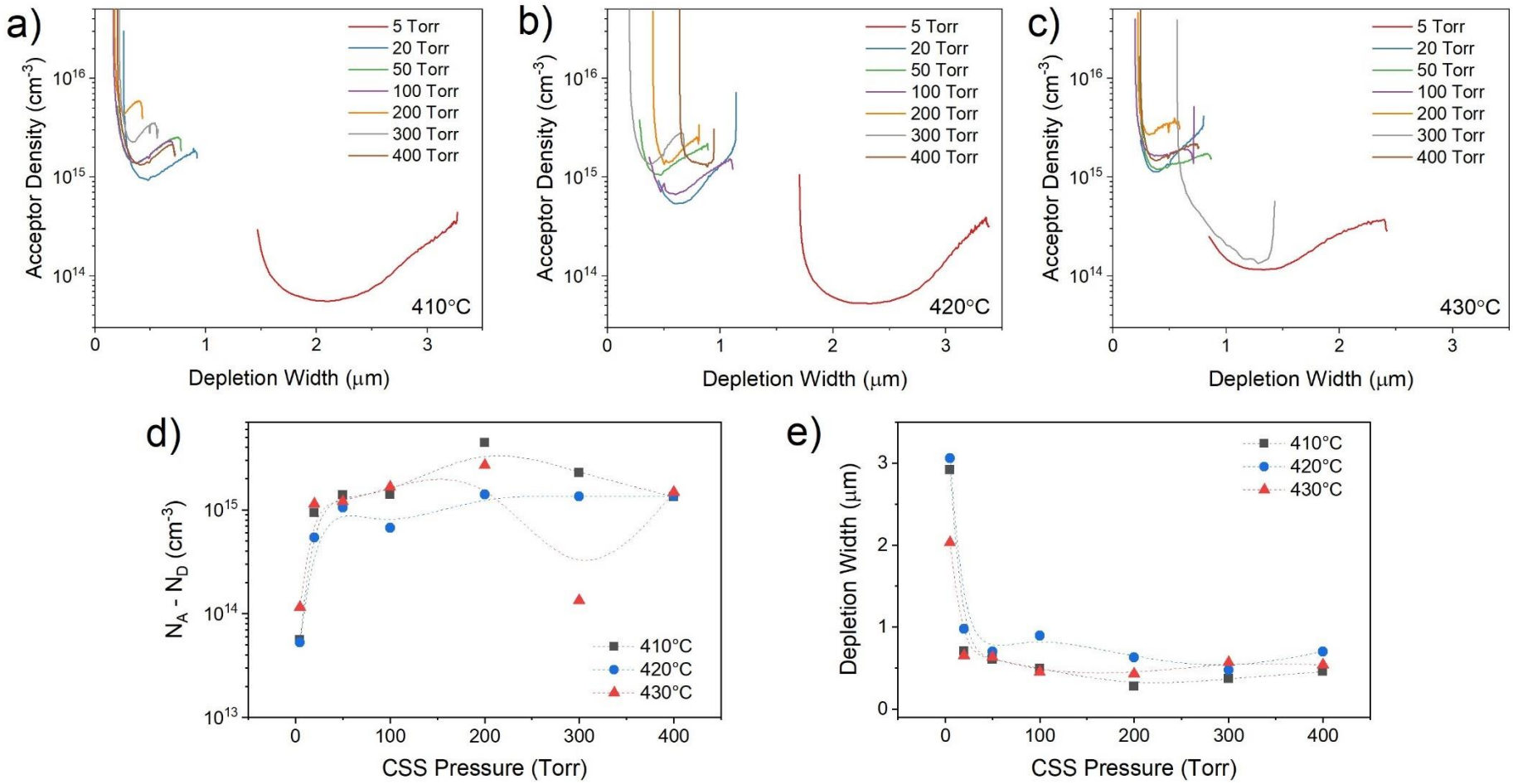

Figure 7.14: Acceptor density profiles for CdTe/SnO_2 solar cells grown under 5 – 400 Torr nitrogen and $MgCl_2$ treated at 410°C (a), 420°C (b) and 430°C (c), with the acceptor density estimated from the minima of each curve shown as a function of pressure (d) and depletion width at zero bias shown in (e)

7.3.5 Summary of findings for SnO_2/CdTe solar cells

CdTe films were deposited onto SnO_2 coated substrates and processed into solar cells to enable a comparison with the more common CdS/CdTe device structure. The average grain size was found to be much less sensitive to growth pressure than for CdS substrates, and whilst all films retain a [111] preferential orientation, the texture coefficient shows no systematic variation. XRD measurements indicate strained growth of CdTe when deposited onto SnO_2. This is presumably due to the lattice mismatch between the two layers which remains due to a lack of interdiffusion which was observed for growth on CdS. This strain is relieved to some extent at higher growth pressures, however this is accompanied by increasingly poor substrate coverage causing films grown at 400 Torr to transmit ~1.5% of above band gap light despite an average CdTe film thickness of 7 μm.

Device performance was compared for samples grown at varied pressure and $MgCl_2$ treated between 410°C – 430°C. Treatment at 410°C, which was found to be optimal for CdS/CdTe devices, produces poor device efficiency and low fill factor regardless of growth pressure. This is due to 'S' shaped *JV* curves which indicate poor conduction alignment, resulting in a spike-like barrier to photogenerated electrons similar to that reported for CdTe based devices with MZO window layers. This was overcome by increasing the $MgCl_2$ treatment temperature up to 430°C, demonstrating that the SnO_2/CdTe device structure is not only tolerant to higher treatment temperatures, but requires them to achieve reasonable performance. Low growth pressures were found to result in the highest device efficiency, with decreasing shunt resistance at higher pressure due to poor substrate coverage. EQE measurements show improved collection efficiency compared to CdS/CdTe devices, particularly in the blue response due to the higher band gap of SnO_2. Despite this, the short circuit current density was not significantly improved due to the presence of a secondary barrier at the SnO_2 interface which is reduced, but not eliminated by high temperature $MgCl_2$ treatment. The doping density of all devices grown above 5 Torr was around ~10^{15} cm^{-3} irrespective of growth pressure or treatment temperature, which is encouraging considering the lack of intentional extrinsic dopants incorporated into the absorber layer. This is higher than measured for growth on CdS and could indicate a less complex defect structure that is mor amenable to achieving high doping densities.

Despite the increased transparency of the window layer and relatively high doping density achieved for some cells, this device structure remains limited by a charge transport barrier and poor growth of CdTe on the underlying SnO_2 substrate. The incorporation of a CdSe layer between SnO_2 and CdTe is investigated in the next section in an attempt to overcome this.

7.4 $CdSe_xTe_{1-x}$ solar cells with a SnO_2 window layer

7.4.1 Introduction

It has been seen in the previous section that the efficiency of SnO_2/CdTe solar cells is limited by poor band alignment indicated by 'S' shaped *JV* curves. The use of higher temperatures than normal during $MgCl_2$ treatment can overcome this to some extent, however a barrier to photocurrent is likely to persist regardless of processing conditions. Recent advances for CdTe based solar cells with a selenium graded absorber layer have resulted in improved carrier lifetime and increased V_{bi} [39,40], and may also offer a route to an improved band alignment. The CdTe band gap was varied in this section by alloying with CdSe to produce a $CdSe_xTe_{1-x}$ layer. As CdSe is alloyed with CdTe both the CBM and VBM shift downwards, and the band gap is decreased via the band bowing effect for low selenium compositions [41]. Both effects would be expected to increase the electron affinity of $CdSe_xTe_{1-x}$ and will therefore have an impact on the band alignment with SnO_2.

$CdSe_xTe_{1-x}$ layers can be deposited directly via CSS [42], but are more commonly are formed by sequentially depositing CdSe and CdTe layers which intermix during annealing [43,44]. Whilst depositing a separate CdSe layer might pose issues such as Kirkendall voiding [45], it avoids the requirement to build custom deposition equipment and efficiencies above 19% have been obtained [11] indicating this is a feasible approach. Furthermore, as Figure 7.10 indicates that growth of CdTe directly onto SnO_2 substrates is hindered by incomplete coverage, the same might be expected for $CdSe_xTe_{1-x}$. Depositing onto CdSe instead might alleviate this.

7.4.2 Device fabrication

A further set of 21 devices were fabricated on TEC15M substrates in a similar manner to those described in section 7.3.2, with 100 nm CdSe deposited prior to CdTe growth. CdSe was deposited onto seven 5×5 cm^2 TEC15M substrates by sputtering at a power density of 1.32 W/cm^2 and substrate temperature of 200°C under 5 mTorr Ar. CdTe was then deposited at varying nitrogen pressures between 5 – 400 Torr, whereby the growth time adjusted to achieve an average thickness of ~7 μm in each case (Table 7.2). All further device processing was carried out as previously described in section 7.2.2. Interdiffusion of the CdSe and CdTe layers is expected to occur during CSS deposition, whereby the substrate temperature is maintained at 550°C for between 4 – 162 min depending on the growth pressure, and during the $MgCl_2$ treatment which takes place at 410°C – 430°C for 20 mins. The level of interdiffusion and therefore thickness and composition of the resulting $CdSe_xTe_{1-x}$ layer will therefore vary between samples depending on processing conditions.

7.4.3 Structural analysis of CdTe films deposited on CdSe at varied pressure

Figure 7.15(a-g) shows SEM images of the back surface of as-deposited CdTe films grown under nitrogen pressures between 5 – 400 Torr onto CdSe coated TEC15M substrates. The grain size distribution is inset for each micrograph, showing the equivalent radius of >200 grains for each growth pressure as determined from the grain area. The average grain radius is also plotted as a function of growth pressure in Figure 7.15h. Low pressure (i.e. 5 Torr) growth results in films with a hexagonal grain structure covering a more compact underlayer of tightly packed grains. The grain size is relatively uniform with average radius of 1.2 μm. As the growth pressure is increased, the grain structure becomes more faceted with a smoother surface. Grain size increases slightly up to 200 Torr reaching an average radius of 1.6 μm, although many small grains remain and histograms become increasingly skewed. Average grain size remains constant at growth pressures above 200 Torr, whilst the grains shape becomes more irregular with sharp, well-defined crystal facets.

The variation of morphology with growth pressure of CdTe films grown on CdSe is broadly similar to those grown on CdS (Figure 7.1), as might be expected given the similar crystal structure of both substrates. The hexagonal facets indicative of [111] oriented grains deposited at low pressure are more rounded for CdTe grown on CdSe in comparison to those deposited on CdS, which is known to template growth in the [111] direction to some extent [30]. The grain size of films grown on CdSe substrates (Figure 7.15h) is smaller than for CdS substrates (Figure 7.1h), which is consistent with comparisons from EBSD measurements [45], and shows less variation with growth pressure.

The average grain size for CdTe films grown on CdSe/SnO_2 substrates increases with growth pressure up to 200 Torr, which is not observed as clearly for growth directly onto SnO_2. The grain size with CdSe/SnO_2 is also consistently lower for all growth pressures. The addition of CdSe between the SnO_2 and CdTe layer therefore has a significant impact on the growth dynamics. Whereas CdTe/SnO_2 films grown at high pressures showed visibly poor substrate coverage with a high pinhole density, confirmed by SEM and UV-vis measurements, there is no evidence of poor growth for these films. This suggests that depositing CdSe/CdTe bilayers is an effective method of improving the film quality when using SnO_2 substrates that is distinct from the benefits achieved from band gap grading a defect passivation [39,46]. It is unclear whether direct deposition of $CdSe_xTe_{1-x}$ would be affected by poor quality growth on SnO_2 as found for CdTe, but a CdSe interlayer could be a similarly viable strategy to overcome this. Whilst Kirkendall voiding is likely to be an issue for such a growth strategy, this could be mitigated by using a thinner CdSe layer to provide a suitable growth surface whilst limiting interdiffusion.

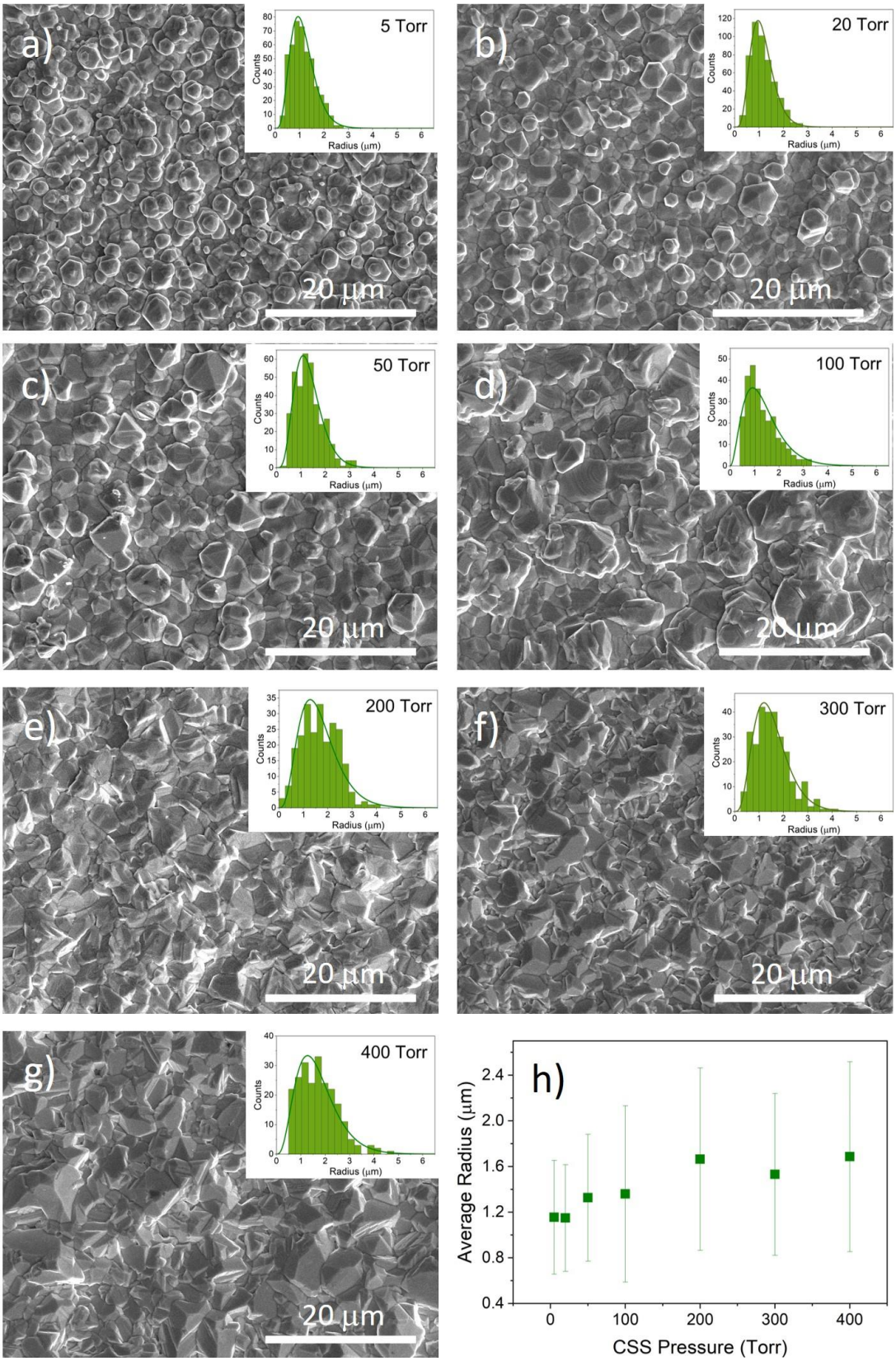

Figure 7.15: SEM images of the back surface of as grown CdTe films deposited on CdSe at pressures between 5 – 400 Torr (a) – (g) with the grain size distribution shown inset, as well as the mean radius plotted as a function of deposition pressure (h)

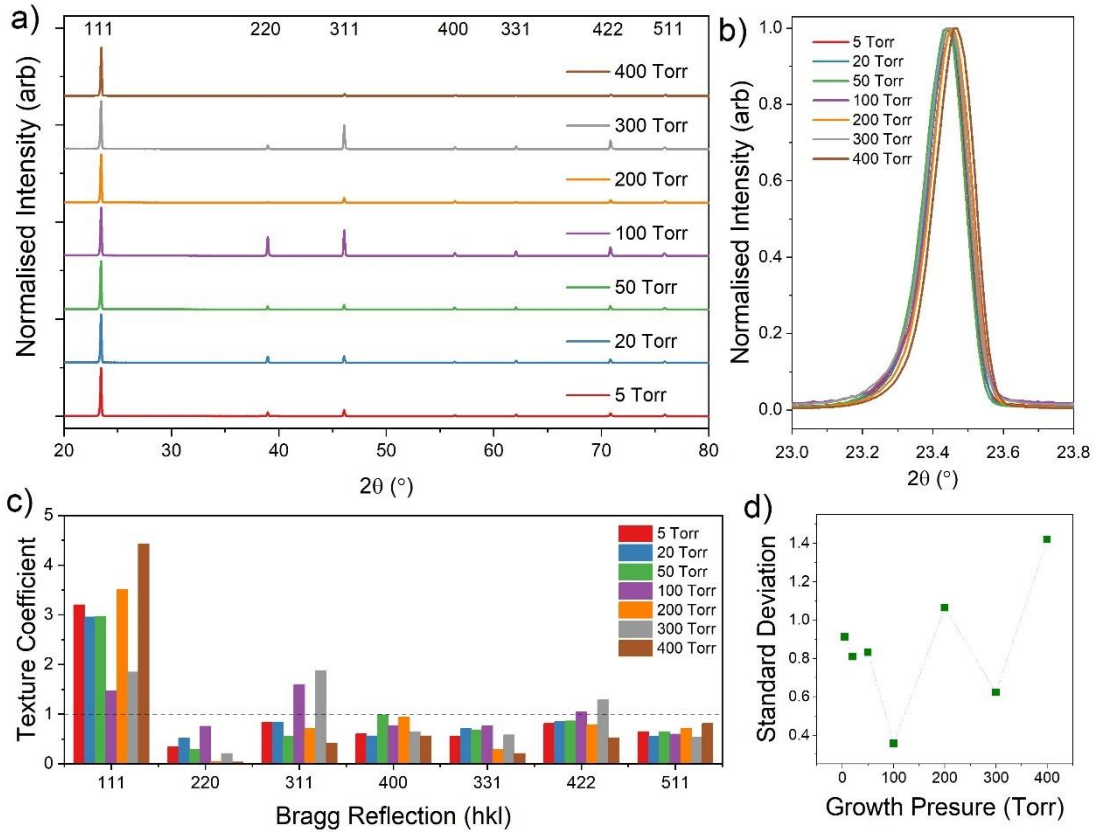

Figure 7.16: XRD data for 7 μm CdTe films grown on CdSe coated substrates under varying pressure of nitrogen (a), with higher magnification of the 111 peak shown in (b). The texture coefficient for each Bragg reflection at each growth pressure is given in (c) as well as the standard deviation of the texture coefficients for each sample in (d)

Figure 7.16 shows XRD patterns for the as grown CdTe films deposited between 5 – 400 Torr onto sputtered CdSe. The mixing enthalpy for all compositions of $CdSe_xTe_{1-x}$ is lower than that of CdTe or CdSe at temperatures above ~168°C [41], and therefore the mixed alloy would be expected to readily form given the substrate temperature of 550°C during CSS deposition. However, these diffraction patterns demonstrate that only a single CdTe phase is measured from the back surface with no sign of a CdSe or $CdSe_xTe_{1-x}$ phase. The dominant peak in each diffraction pattern is the 111 reflection centred around 23.45°, corresponding to a lattice constant of 6.57 Å which is larger than 6.48 Å expected for a powdered sample and literature values for bulk CdTe [46]. This difference likely indicates residual tensile stress in the lattice, which has been found for all CSS grown CdTe samples. There is some indication that the lattice constant decreases with increasing growth pressure as would be expected for increasing selenium content [47], however this is less than the precision afforded by the resolution in diffraction angle and therefore represents only a minor difference. The lack of change with the addition of 100 nm CdSe is likely due to the thick (~7 μm) CdTe film resulting in a very dilute alloy that does not extend throughout the sample in sufficient quantity to be detected, especially given the limited penetration of x-rays into the sample from the surface. It is not

possible to determine from these measurements whether a selenium rich phase exists at the front contact. Control over the selenium composition is especially critical here since $CdSe_xTe_{1-x}$ with $x > 0.3$ can crystalize in the wurtzite structure, which is harmful for photovoltaic applications [43,46]. It is also noteworthy that the texture coefficient does not show a dependence on growth pressure for any of the Bragg peaks, with all films displaying a [111] preferential orientation.

7.4.4 Device analysis of $CdSe_xTe_{1-x}/SnO_2$ solar cells deposited at varied pressure

In addition to modifying the band alignment at the junction interface (section 7.4.1), the addition of selenium is expected to improve long wavelength current collection [44] and induce defect passivation [46], while a graded band gap is expected to produce an internal electric field within the absorber layer. The growth duration, which was varied with growth pressure, as well as the $MgCl_2$ processing temperature is expected to strongly influence the distribution of selenium throughout the device, and therefore requires careful optimisation. Performance parameters taken from *JV* curves of devices with varied growth pressure are shown in Figure 7.17 for $MgCl_2$ activation temperatures of 410°C, 420°C and 430°C. In contrast to SnO_2/CdTe devices, optimal processing conditions for $SnO_2/CdSe_xTe_{1-x}$ devices involve lower temperature $MgCl_2$ treatment, with efficiencies declining for higher temperatures. All performance parameters contribute to this efficiency reduction, which is most noticeable for low growth pressures. Interdiffusion of CdSe into CSS grown CdTe is known to occur during chlorine activation as well as deposition [42], in contrast to CdS where sulphur diffusion primarily takes place during CdTe growth [12]. Therefore the effect of selenium redistribution due to $MgCl_2$ treatment is expected to be most apparent for low growth pressures, as higher pressure growth is accompanied by longer deposition runs which will act to promote interdiffusion prior to the chloride treatment [48].

Figure 7.17 shows that higher pressure growth is seen to be detrimental to device efficiency due to a gradual reduction in both open circuit voltage and fill factor. However, despite this reduction, devices spanning a wide parameter space consisting of 21 processing combinations maintain reasonable performance, even for clearly overtreated cells that were subjected to several hours of high temperature growth conditions. This contrasts with the CdS/CdTe and SnO_2/CdTe devices described previously, where efficiency declines quickly outside of an optimal processing parameter window. Optimised $SnO_2/CdSe_xTe_{1-x}$ devices reached higher efficiencies than the CdS/CdTe and SnO_2/CdTe devices in this study. This is primarily due to

an increase in J_{sc} afforded by a more transparent window layer compared to CdS, whilst retaining high V_{oc} by improving the absorber interface with SnO_2.

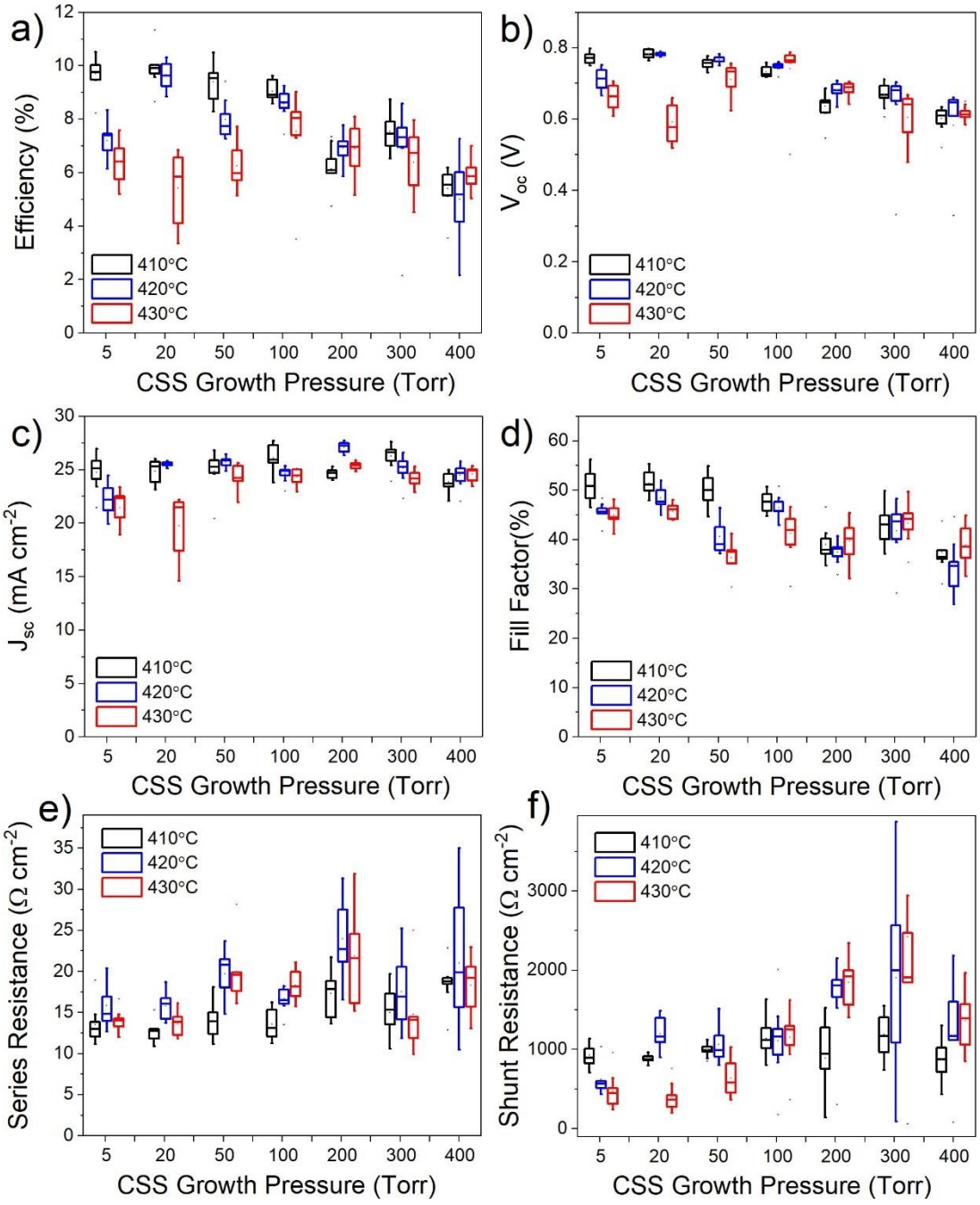

Figure 7.17: Box and whisker plots showing *JV* performance parameters for $SnO_2/CdSe_xTe_{1-x}$ devices grown under 5 - 400 Torr of nitrogen, activated at 410°C, 420°C, 430°C. The box boundaries show the upper and lower quartiles with a horizontal line for the median value, and the range given by the whiskers. The efficiency (a), open circuit voltage (b), short circuit current density (c), fill factor (d), series resistance (e) and shunt resistance (f) is given as a function of growth pressure

Figure 7.18 shows *JV* curves from the highest efficiency cell of each device. There is no sign of an 'S' shape which reduced fill factor for SnO_2/CdTe devices for any of the activation temperatures, indicating an improved band alignment at the front contact. Whilst a small increase in the CBM of CdTe is expected with selenium alloying [24], this would be expected to increase the conduction band offset with SnO_2 and therefore produce a larger barrier to photocurrent. Therefore the improved alignment indicated by the removal of 'S' shaped *JV* curves, even for low $MgCl_2$ temperature activation, is instead likely to result from reduced interfacial defect density either due to selenium induced passivation [46] or less strained growth of CdTe on CdSe instead of directly onto SnO_2. The uniformity of CdTe films has been improved by depositing CdSe onto SnO_2 coated substrates prior to growth, with no evidence of pinholes and negligible above band gap light transmission for all samples, in contrast to when directly deposited onto SnO_2. This allows for shunt resistance to be maintained or increased at higher growth pressures as shown in Figure 7.17f.

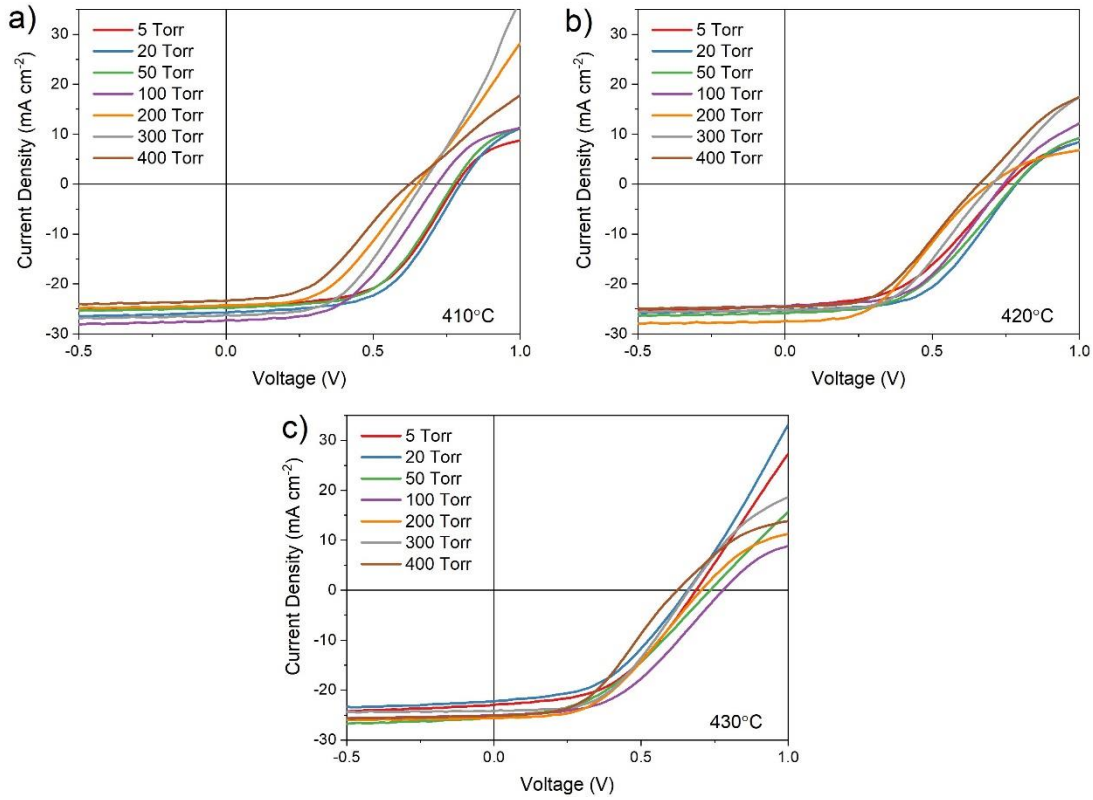

Figure 7.18: *JV* curves for the highest efficiency contact of SnO_2/$CdSe_xTe_{1-x}$ devices grown under varied N_2 pressure and treated at 410°C (a), 420°C (b) and 430°C (c)

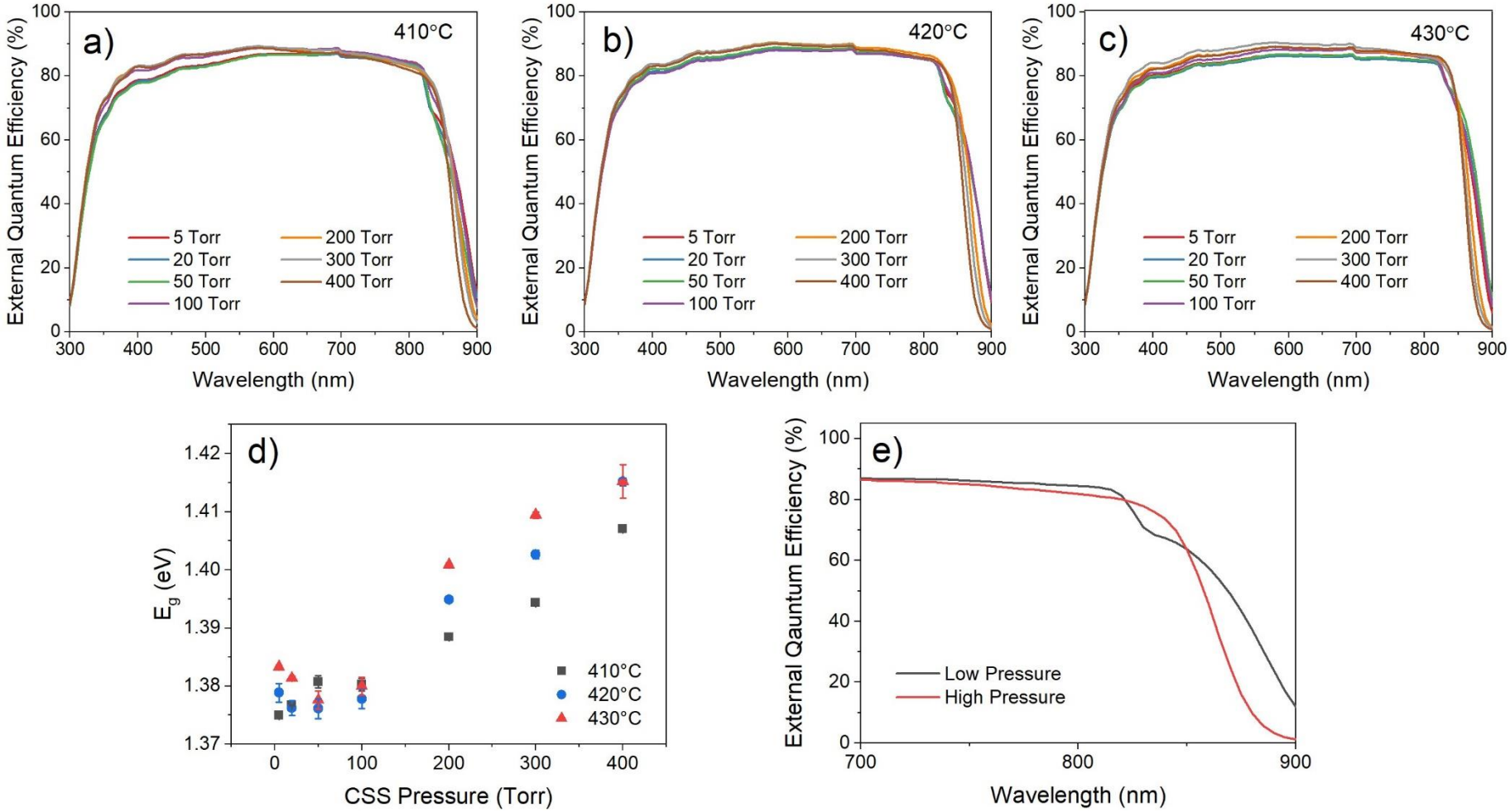

Figure 7.19: EQE spectra for devices grown on SnO_2/CdSe under 5 – 400 Torr nitrogen and subject to $MgCl_2$ treatment at 410°C (a), 420°C (b) and 430°C (c) as well as the minimum absorber band gap (g) and example EQE curves demonstrating the qualitative differences between low (5 Torr) and high (400 Torr) growth pressure on the long wavelength region absorption shoulder (h)

Figure 7.19(a-c) shows EQE measurements for the highest efficiency contacts from each device with varied growth pressure and $MgCl_2$ activation temperature. Whilst there is little systematic variation in the collection efficiency across most wavelengths, there is a noticeable shift in the long wavelength cut-off, which is commonly observed for selenium alloyed CdTe films [49]. This results from the variation in absorber band gap, which is estimated by linear extrapolation of the cut-off to the *x*-axis and shown as a function of pressure for the different treatment temperatures in Figure 7.19g. At low pressures, the band gap of the $CdSe_xTe_{1-x}$ layer is lower than both CdTe (~1.45 eV) and CdSe (~1.7 eV), reaching a minimum of 1.38 eV, which corresponds to a $CdSe_xTe_{1-x}$ layer with a composition of around $x = 0.3$ [41,47]. As the pressure is increased beyond 100 Torr there is an increase in band gap as the selenium content becomes more dilute, with longer growth times encouraging its redistribution. The band gap increases linearly for each $MgCl_2$ activation temperature up to a maximum of 1.41 eV. This remains lower than that of CdTe indicating a selenium rich region remains at the front contact for all devices despite the high mixing enthalpy and long growth times. This may be affected by the larger grain size for high pressure growth restricting selenium diffusion, which has been shown to occur most readily along grain boundaries before migrating to the grain interior [46].

The shape of the EQE response at long wavelength varies with growth pressure for all activation temperatures, with representative example shown in Figure 7.19e for clarity. At low growth pressure, corresponding to a short growth duration, there are two separate absorption onsets from distinct $CdSe_xTe_{1-x}$ and CdTe layers around ~830 nm and ~870 nm respectively. This indicates that whilst the $CdSe_xTe_{1-x}$ layer allows collection deeper into the infrared portion of the solar spectrum, it is too thin to fully absorb the incoming photons and therefore some are transmitted through to the CdTe layer whereby they can be absorbed and collected. As growth pressure is increased, progressively longer deposition times are required for equivalent film thickness which allows further intermixing of the CdSe and CdTe layers. This results in a more dilute selenium concentration in the $CdSe_xTe_{1-x}$ layer and therefore limits the infrared collection. However, as this layer is more dilute and therefore extends further into the absorber layer than for low pressure growth, it can fully absorb the incoming photons resulting in a single absorption onset around 850 nm. This can also be observed to a lesser extent with increasing $MgCl_2$ temperature, and together with Figure 7.19d shows that the distribution of selenium is clearly influenced by both CSS deposition conditions and chlorine processing, in contrast to CdS/CdTe devices where sulphur distribution occurs primarily during CSS deposition [12].

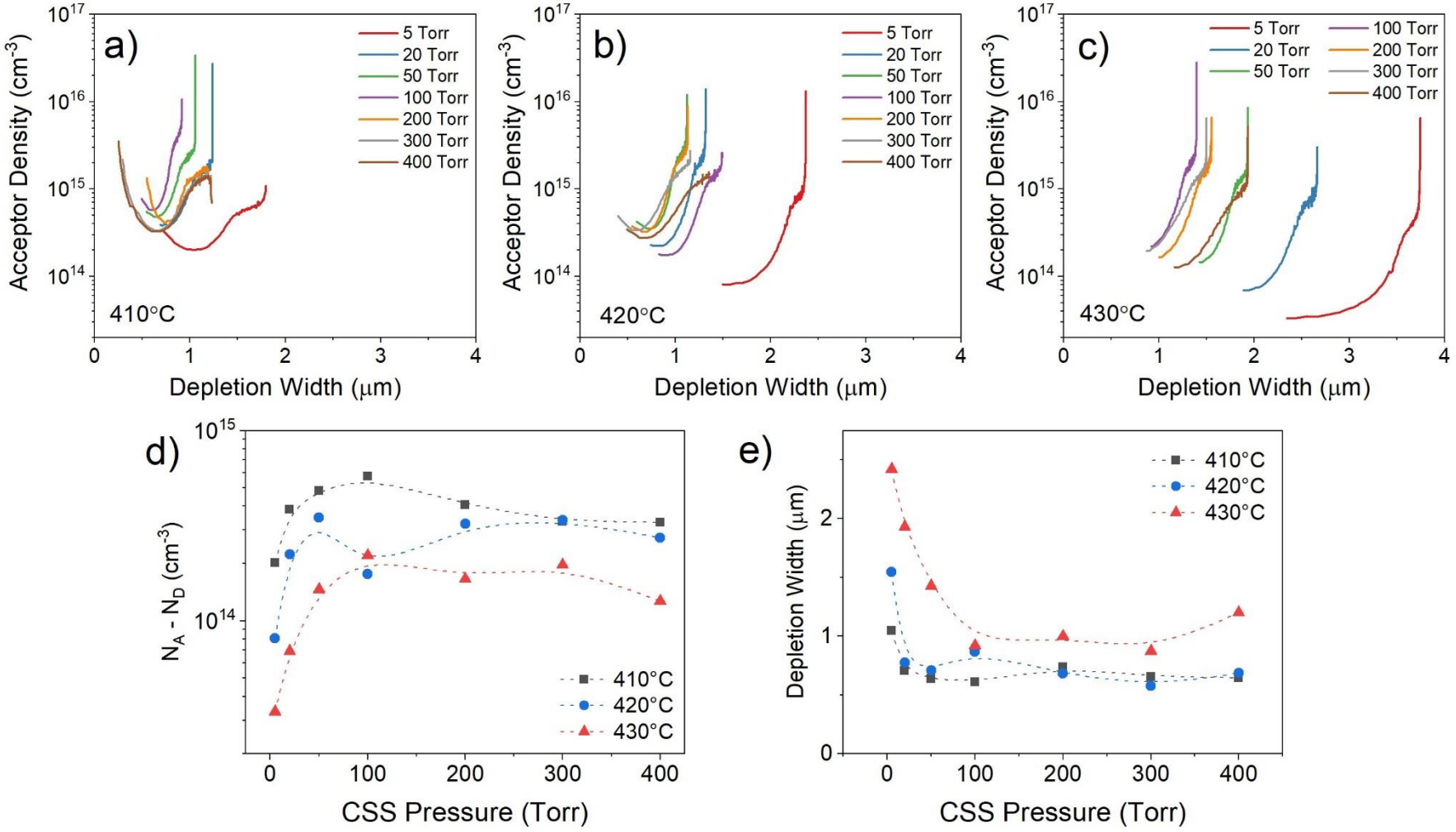

Figure 7.20: Acceptor density profiles for $SnO_2/CdSe_xTe_{1-x}$ solar cells grown under 5 – 400 Torr nitrogen and $MgCl_2$ treated at 410°C (a), 420°C (b) and 430°C (c), with the net acceptor density estimated from the minima of each curve shown as a function of pressure (d) and depletion width at zero bias shown in (e)

Figure 7.20(a-c) shows acceptor density – depletion width plots for devices different growth pressure at three $MgCl_2$ treatment temperatures, calculated from *CV* measurements of the highest efficiency contact from each device. The bulk carrier concentration was estimated for each of these from the curve minima and the depletion width was measured at 0 V bias, shown as a function of growth pressure for activation temperatures of 410°C, 420°C and 430°C in Figure 7.20(d-e). As with SnO_2/CdTe devices there is a sharp increase in doping density at growth pressures above 5 Torr before reaching a plateau. This may be due to out-diffusion of impurities from the underlying substrate acting as *p*-type dopants, thereby increasing the net doping density until an equilibrium is reached where they are equally likely to occupy substitutional sites as interstitial sites.

Carrier concentration for these devices is dependent on $MgCl_2$ activation temperature in a similar manner to that for CdS/CdTe devices and in contrast to SnO_2/CdTe devices. Higher $MgCl_2$ activation temperatures result in a wider variation in carrier concentration between films growth at low and high pressure growth than for low activation temperature. The carrier concentration decreases as the $MgCl_2$ processing temperature is increased and the devices become increasingly overtreated, with optimum conditions resulting in a carrier concentration of 5×10^{14} cm^{-3}, around half of that achieved for SnO_2/CdTe devices. This difference between CdTe and $CdSe_xTe_{1-x}$ devices agrees with previous reports which indicate lower doping densities as the selenium content of the alloyed material increases in both thin films [47] and single crystals [50]. This is ascribed to the decreased lattice constant altering the size mismatch between the dopant and host site, which modifies both the solubility and formation energy of acceptor like defects [51]. A similar effect might be the cause of the reduced carrier concentration observed here.

7.4.5 Summary of findings for SnO_2/$CdSe_xTe_{1-x}$ solar cells

A CdSe interlayer between CdTe deposited onto SnO_2 coated substrates has been found to be an effective strategy to improve substrate coverage, whilst also producing a graded $CdSe_xTe_{1-x}$ layer which improves photovoltaic performance. The SnO_2/$CdSe_xTe_{1-x}$ interface was found to be superior to that of SnO_2/CdTe, showing no evidence of 'S' shaped *JV* curves indicative of a conduction band charge transport barrier. This device structure leads to an improved J_{sc} compared to CdS/CdTe and SnO_2/CdTe devices whilst retaining high V_{oc}. Reasonable performance was achieved over a wide range of processing conditions, with low temperature $MgCl_2$ processing and low pressure growth found to be optimal. Interdiffusion occurs during both CSS deposition and $MgCl_2$ treatment, and it is therefore difficult to isolate the impact of

the grading profile from the effect of these processing conditions on the other optoelectronic properties such as doping density and film quality .

7.5 Conclusion

This chapter has studied three device architectures to determine the optimal processing conditions and compare the effectiveness of each. CdTe is initially grown on CdS substrates before being replaced with SnO_2 as a more transparent window layer, and eventually incorporating a selenium graded absorber layer by depositing CdTe onto a CdSe/SnO_2 bilayer. For each structure, the absorber growth pressure was varied between 5 – 400 Torr, and the structural properties of the as grown material compared. These films were then processed into solar cells, using $MgCl_2$ activation temperatures between 410°C – 430°C, which allows for a direct, statistical comparison of device performance across 63 processing conditions.

The CdS/CdTe device structure has been standard for over 40 years, however is limited by a low band gap window layer which causes parasitic absorption. Control over the absorber grain size has been demonstrated by varying the growth pressure during CSS deposition of the CdTe layer, which in turn regulates the adatom arrival rate during deposition and therefore the nucleation kinetics. Although high pressure growth was shown to increase the average CdTe grain size, the extended duration of the high temperature deposition also results in excessive intermixing of the CdS and CdTe layers. High temperature $MgCl_2$ treatments resulted in reduced carrier concentration and poor device performance. Therefore this device structure is limited by the thermal budget available during processing without causing excessive interdiffusion.

SnO_2/CdTe devices benefit from a more transparent window layer allowing more photons to reach the absorber layer and does not interdiffuse during high temperature processing. However, the CdTe films grown directly onto SnO_2 were found to be of poor quality. Strain in the CdTe layer is relaxed to some extent by increasing the growth pressure, however this was found to also result in poor coverage, leaving areas of exposed substrate and therefore offering shunting pathways. Notably, the grain size and texture of these CdTe films were not found to be strongly correlated with growth pressure as for CdS/CdTe films. Devices were also found to be very sensitive to the $MgCl_2$ treatment temperature. Low temperature (410°C) treatment produced poor device efficiency due to ‘S’ shaped *JV* curves, which severely limits fill factor and indicates charge accumulation at the interface due to a transport barrier in the conduction band. This is alleviated by increasing the $MgCl_2$ treatment temperature up to 430°C, causing a substantial increase in efficiency. However, the V_{oc} of SnO_2/CdTe devices

remains lower than for CdS/CdTe indicating inferior junction quality, with no increase in J_{sc} despite the more transparent window layer.

By depositing CdTe onto CdSe/SnO_2 bilayers, the growth surface is changed whilst also having the effect of incorporating selenium into the absorber layer. This allows for improved substrate coverage in comparison to direct deposition onto SnO_2, leading to uniform films without pinholes. Since the CdSe and CdTe layers readily intermix during film growth, a graded $CdSe_xTe_{1-x}$ layer is produced which has a lower band gap than CdTe and forms a junction with SnO_2. The smaller band gap allows for increased current collection, resulting in higher J_{sc}, with V_{oc} similar to that of CdS/CdTe devices and higher than SnO_2/CdTe devices. No evidence of a charge transport barrier was observed for any SnO_2/$CdSe_xTe_{1-x}$ devices, suggesting an improved band alignment compared to SnO_2/CdTe. Whilst reasonable efficiencies were obtained over a wide parameter space with this device structure, interdiffusion occurs during both the absorber deposition and $MgCl_2$ treatment which is expected to significantly impact device performance. Therefore, using this approach it was not possible to disentangle the effect of the selenium grading profile from other changes within the device which occur simultaneously, such as grain size and defect passivation.

The SnO_2/$CdSe_xTe_{1-x}$ device structure combines a wide band gap window layer with a lower band gap absorber layer, allowing the J_{sc} of devices to be improved whilst retaining similar V_{oc} to the more traditional CdS/CdTe device structure. Whilst some control over the microstructure of $CdSe_xTe_{1-x}$ is afforded by changing the growth pressure, the maximum grain size observed in this study remains below the film thickness, leading to a high density of grain boundaries within the absorber layer. However, further investigations into the effect of the window layer on the early stage nucleation and growth of CdTe would be beneficial in determining optimal processing parameters to produce large grained, high quality absorber layers. A large, well oriented grain structure would result in fewer high angle grain boundaries, especially those running parallel to the junction. The effect of substrate properties such as roughness, chemistry, pre-treatments, and passivation layers also offer potential avenues of investigation.

7.6 References

1. Klenk, R. Characterisation and modelling of chalcopyrite solar cells. *Thin Solid Films* **387**, 135–140 (2001).
2. Kartopu, G. *et al.* Effect of window layer composition in Cd_{1-x} Zn_xS/CdTe solar cells. *Progress in Photovoltaics: Research and Applications* **22**, 18–23 (2014).
3. McCandless, B. E., Moulton, L. V. & Birkmire, R. W. Recrystallization and sulfur diffusion in $CdCl_2$-treated CdTe/CdS thin films. *Progress in Photovoltaics: Research and Applications* **5**, 249–260 (1997).
4. Kephart, J. M. *et al.* Band alignment of front contact layers for high-efficiency CdTe solar cells. *Solar Energy Materials and Solar Cells* **157**, 266–275 (2016).
5. Wu, X. *et al.* Nanostructured CdS:O film: preparation, properties, and application. *physica status solidi (c)* **1**, 1062–1066 (2004).
6. Kephart, J. M., Geisthardt, R. M. & Sampath, W. S. Optimization of CdTe thin-film solar cell efficiency using a sputtered, oxygenated CdS window layer. *Progress in Photovoltaics: Research and Applications* **23**, 1484–1492 (2015).
7. Li, D. B. *et al.* Eliminating S-kink to maximize the performance of MgZnO/CdTe solar cells. *ACS Applied Energy Materials* **2**, 2896–2903 (2019).
8. Artegiani, E. *et al.* Analysis of magnesium zinc oxide layers for high efficiency CdTe devices. *Thin Solid Films* **672**, 22–25 (2019).
9. Ren, S. *et al.* Rapid thermal annealing on ZnMgO window layer for improved performance of CdTe solar cells. *Solar Energy Materials and Solar Cells* **187**, 97–103 (2018).
10. Bittau, F. *et al.* Degradation of Mg-doped zinc oxide buffer layers in thin film CdTe solar cells. *Thin Solid Films* **691**, 137556 (2019).
11. Ablekim, T. *et al.* Thin-film solar cells with 19% efficiency by thermal evaporation of CdSe and CdTe. *ACS Energy Letters* 892–896 (2020).
12. Taylor, A. A. *et al.* A comparative study of microstructural stability and sulphur diffusion in CdS/CdTe photovoltaic devices. *Solar Energy Materials and Solar Cells* **141**, 341–349 (2015).
13. Romeo, A., Bätzner, D. L., Zogg, H. & Tiwari, A. N. Recrystallization in CdTe/CdS. *Thin Solid Films* **361**, 420–425 (2000).
14. Amarasinghe, M. *et al.* Influence of CdTe Deposition Temperature and Window Thickness on CdTe Grain Size and Lifetime after CdCl 2 Recrystallization. *IEEE Journal of Photovoltaics* **8**, 600–603 (2018).
15. Major, J. D., Proskuryakov, Y. Y., Durose, K., Zoppi, G. & Forbes, I. Control of grain size in sublimation-grown CdTe, and the improvement in performance of devices with systematically increased grain size. *Solar Energy Materials and Solar Cells* **94**, 1107–1112 (2010).
16. Bosio, A., Romeo, N., Mazzamuto, S. & Canevari, V. Polycrystalline CdTe thin films for photovoltaic applications. *Progress in Crystal Growth and Characterization of Materials* **52**, 247–279 (2006).
17. Venables, J. A. *Introduction to Surface and Thin Film Processes*. *Introduction to Surface and Thin Film Processes* (Cambridge University Press, 2000).

18. Albin, D. S., Yan, Y. & Al-Jassim, M. M. The effect of oxygen on interface microstructure evolution in CdS/CdTe solar cells. *Progress in Photovoltaics: Research and Applications* **10**, 309–322 (2002).

19. Shen, K. *et al.* High efficiency CdTe solar cells with a through-thickness polycrystalline CdTe thin film. *RSC Advances* **6**, 52326–52333 (2016).

20. Barna, Á., Barna, P. B., Radnóczi, G., Reicha, F. M. & Tóth, L. Formation of aluminium thin films in the presence of oxygen and nickel. *Physica Status Solidi (a)* **55**, 427–435 (1979).

21. Petrov, I., Barna, P. B., Hultman, L. & Greene, J. E. Microstructural evolution during film growth. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **21**, S117–S128 (2003).

22. Durose, K. & Russell, G. J. Twinning in CdTe. *Journal of Crystal Growth* **101**, 246–250 (1990).

23. Abbas, A. *et al.* Cadmium chloride assisted re-crystallization of CdTe: The effect of annealing over-treatment. in *2014 IEEE 40th Photovoltaic Specialist Conference, PVSC 2014* 701–706 (2014).

24. Wei, S. H., Zhang, S. B. & Zunger, A. First-principles calculation of band offsets, optical bowings, and defects in CdS, CdSe, CdTe, and their alloys. *Journal of Applied Physics* **87**, 1304–1311 (2000).

25. Major, J. D. & Durose, K. Early stage growth mechanisms of CdTe thin films deposited by close space sublimation for solar cells. *Solar Energy Materials and Solar Cells* **95**, 3165–3170 (2011).

26. Strauss, A. J. The physical properties of cadmium telluride. *Revue de Physique Appliquée* **12**, 167–184 (1977).

27. Neretina, S. *et al.* The role of lattice mismatch in the deposition of CdTe thin films. *Journal of Electronic Materials* **35**, 1224–1230 (2006).

28. Terheggen, M. *et al.* Analysis of bulk and interface phenomena in CdTe/CdS thin-film solar cells. in *Interface Science* vol. 12 259–266 (Springer, 2004).

29. Perkins, C. L., McGott, D. L., Reese, M. O. & Metzger, W. K. SnO_2-catalyzed oxidation in high-efficiency CdTe solar cells. *ACS Applied Materials and Interfaces* **11**, 13003–13010 (2019).

30. Siepchen, B., Klein, A. & Jaegermann, W. Interface formation in CdTe solar cells: Nucleation of CdTe on CdS(0001) and (10$\bar{1}$0). *physica status solidi (RRL) - Rapid Research Letters* **2**, 169–171 (2008).

31. Saive, R. S-shaped current-voltage characteristics in solar cells: a review. *IEEE Journal of Photovoltaics* **9**, 1477–1484 (2019).

32. Islam, M. N. & Hakim, M. O. Electron affinity and work function of polycrystalline SnO_2 thin film. *Journal of Materials Science Letters* **5**, 63–65 (1986).

33. Zhang, D. & Dong, S. Challenges in band alignment between semiconducting materials: A case of rutile and anatase TiO_2. *Progress in Natural Science: Materials International* vol. 29 277–284 (2019).

34. Butler, K. T., Buckeridge, J., Catlow, C. R. A. & Walsh, A. Crystal electron binding energy and surface work function control of tin dioxide. *Physical Review B - Condensed Matter and Materials Physics* **89**, 115320 (2014).

35. Klein, A. *et al.* Surface potentials of magnetron sputtered transparent conducting oxides. *Thin Solid Films* **518**, 1197–1203 (2009).

36. Batzill, M. & Diebold, U. The surface and materials science of tin oxide. *Progress in Surface Science* vol. 79 47–154 (2005).

37. Scheer, R. & Schock, H.-W. Appendix A: Frequently Observed Anomalies. in *Chalcogenide Photovoltaics* 305–314 (Wiley-VCH Verlag GmbH & Co. KGaA, 2011). doi:10.1002/9783527633708.ch7.

38. Yang, J.-H., Yin, W.-J., Park, J.-S., Ma, J. & Wei, S.-H. Review on first-principles study of defect properties of CdTe as a solar cell absorber. *Semiconductor Science and Technology* **31**, 083002 (2016).

39. Munshi, A. H. *et al.* Polycrystalline CdSeTe/CdTe absorber cells with 28 mA/cm^2 short-circuit current. *IEEE Journal of Photovoltaics* **8**, 310–314 (2018).

40. Zheng, X. *et al.* Recombination and bandgap engineering in CdSeTe/CdTe solar cells. *APL Materials* **7**, 071112 (2019).

41. Yang, J. & Wei, S.-H. First-principles study of the band gap tuning and doping control in $CdSe_xTe_{1-x}$ alloy for high efficiency solar cell. *Chinese Phys. B* **28**, 086106 (2019).

42. Munshi, A. H. *et al.* Effect of $CdCl_2$ passivation treatment on microstructure and performance of CdSeTe/CdTe thin-film photovoltaic devices. *Solar Energy Materials and Solar Cells* **186**, 259–265 (2018).

43. Poplawsky, J. D. *et al.* Structural and compositional dependence of the $CdTe_xSe_{1-x}$ alloy layer photoactivity in CdTe-based solar cells. *Nature Communications* **7**, 1–10 (2016).

44. Paudel, N. R. & Yan, Y. Enhancing the photo-currents of CdTe thin-film solar cells in both short and long wavelength regions. *Applied Physics Letters* **105**, 183510 (2014).

45. Baines, T., Bowen, L., Mendis, B. G. & Major, J. D. Microscopic Analysis of Interdiffusion and Void Formation in $CdTe_{(1-x)}Se_x$ and CdTe Layers. *ACS Applied Materials and Interfaces* **12**, 38070–38075 (2020).

46. Fiducia, T. A. M. *et al.* Understanding the role of selenium in defect passivation for highly efficient selenium-alloyed cadmium telluride solar cells. *Nature Energy* **4**, 504–511 (2019).

47. Lingg, M. *et al.* Structural and electronic properties of $CdTe_{1-x}Se_x$ films and their application in solar cells. *Science and Technology of Advanced Materials* **19**, 683–692 (2018).

48. Baines, T. *et al.* Incorporation of CdSe layers into CdTe thin film solar cells. *Solar Energy Materials and Solar Cells* **180**, 196–204 (2018).

49. Swanson, D. E., Sites, J. R. & Sampath, W. S. Co-sublimation of $CdSe_xTe_{1-x}$ layers for CdTe solar cells. *Solar Energy Materials and Solar Cells* **159**, 389–394 (2017).

50. Nagaoka, A., Nishioka, K., Yoshino, K., Kuciauskas, D. & Scarpulla, M. A. Growth and characterization of arsenic-doped $CdTe_{1-x}Se_x$ single crystals grown by the Cd-solvent traveling heater method. *Journal of Electronic Materials* **49**, 6971–6976 (2020).

51. Ma, J. & Wei, S. H. Bowing of the defect formation energy in semiconductor alloys. *Physical Review B - Condensed Matter and Materials Physics* **87**, 241201 (2013).

Chapter 8

Conclusions and further work

8.1 Summary of research outcomes

The aim of this thesis was to investigate alternative device structures for CdTe based solar cells and explore new avenues to improve performance. Over the course of this work, each of the key layers in the standard CdS/CdTe device architecture have been either replaced or modified, and the effect this has on device performance has been characterised. In chapter 5, a range of organic compounds have been assessed as potential contact layers in an attempt to facilitate hole extraction, serving a similar purpose as the more commonly used inorganic contact layers such as ZnTe or MoO_x which are often included in CdTe device stacks. Chapter 6 investigated the effect of incorporating NaF into the absorber layer, either as a pre-metallisation doping step in a similar approach to how Cu is commonly incorporated, or as an additive in the $MgCl_2$ activation treatment. The use of SnO_2 as an alternative widow layer to CdS is explored briefly in chapter 6 and more fully in chapter 7. A low band gap $CdSe_xTe_{1-x}$ phase was also introduced at the front interface to establish a selenium graded absorber layer and paired with an SnO_2 window layer. A comprehensive study of device processing with and without this selenium grading is presented in chapter 7, which includes a comparison to the more typical CdS/CdTe device architecture. The results of each of these investigations are presented in the relevant chapters, and the main findings are briefly summarised below.

In chapter 5, three organic compounds, P3HT, spiro-OMeTAD and PFO, were spin coated onto the back surface of CdTe solar cells prior to metallisation with Au. After optimising the processing conditions for each device structure, the organic contact layers were compared against each other and a device with a simple Au-only contact. The inclusion of all organic layers resulted in lower peak performance, irrespective of processing conditions. In the case of P3HT and spiro-OMeTAD, this reduction was a minor effect, however devices with PFO had significantly lower peak efficiency due to increased series resistance. Temperature dependent *JV* measurements were used to determine the Schottky barrier height at the back

contact for each device structure. All three organic contacts resulted in a lower barrier height, and both P3HT and PFO were particularly effective. However, these devices showed lower efficiency that the Au-only device despite the lower barrier height due to the inclusion of an additional layer and the associated increase in series resistance.

Whilst the organic contacts did not result in an improvement in peak efficiency, all three device structures showed a higher average efficiency compared to the control device. This was attributed to the organic layers acting to block pinholes in the absorber layer, therefore preventing areas with a poor diode response from drastically reducing device performance. By comparing the performance of individual cells as a function of absorber layer thickness, it is clear that devices with an organic contact layer are much more tolerant of thin absorber layers that would otherwise lead to low efficiency due an increased pinhole density. P3HT and PFO were equally effective at blocking pinholes, whilst devices with spiro-OMeTAD were slightly less so. The effectiveness of a pinhole blocking layer is likely to be determined in part by its conductivity, and therefore the dopants included to increase the performance of devices with a spiro-OMeTAD layer may also reduce its pinhole blocking ability.

In chapter 6, NaF was incorporated into the absorber layer of devices to study the effect of sodium, which is expected to be a common impurity, and to assess its effectiveness as a *p*-type dopant in CdTe. Initially, a 1 nm layer of NaF was deposited onto the back surface of $MgCl_2$ treated devices following etching, and annealed at temperatures up to 350°C. Sodium was found to be highly mobile in CdTe, and present in all devices irrespective of NaF deposition due to unintentional impurities. Diffusion of Na away from the back surface where it was deposited occurred predominantly along grain boundaries at low anneal temperatures (200°C) and into the grain interior at higher temperature (300°C). This proved to be an effective route to increasing the bulk doping density of the CdTe layer and appears to aid the formation of a low resistance back contact. None of the devices with NaF displayed rollover in forward bias, implying a reduced barrier height compared to the control device. Despite this, the efficiency of devices with an NaF layer were not significantly higher than those without, as the annealing step required to effectively redistribute sodium into the device also leads to oxidation of the back surface which thereby increases series resistance.

An alternative route to incorporating sodium into the device structure was adopted by evaporating NaF prior to the $MgCl_2$ treatment. This was found to enhance the aggressive recrystallization of CdTe layers deposited via sputtering at low substrate temperature. However, CdTe layers deposited via CSS had a much larger as deposited grain structure which was stable against the subsequent sodium enhanced recrystallization. A series of CdS/CdTe

devices were treated with up to 20 nm NaF deposited prior to activation. Whilst the CdTe layer itself showed no morphological changes upon combined NaF and $MgCl_2$ treatment, the CdS layer recrystallized significantly. This led to a non-continuous window layer which resulted in progressively lower device efficiency as NaF thickness was increased. Tellurium was also found to precipitate out of the CdTe layer and form crystalline regions, which may also contribute to a lower shunt resistance. A further series of SnO_2/CdTe devices were processed, removing the CdS to assess the potential of a combined NaF and $MgCl_2$ treatment with a more robust window layer. These devices did not show deterioration in the SnO_2 layer and benefitted overall from the addition of NaF to the activation treatment. An increase in the acceptor density by an order of magnitude, up to ~10^{15} cm^{-3}, was observed and all devices showed an improvement in V_{oc} compared to the control device. However, the inclusion of excessive NaF during $MgCl_2$ activation results in delamination of the CdTe layer from the underlying SnO_2 and oxidation of the back surface. Despite the low absolute efficiency of these devices, the relative increase upon NaF inclusion indicates this may be a promising route to incorporate sodium and improve the chlorine activation treatment.

In chapter 7, the standard CdS/CdTe device structure was compared to SnO_2/CdTe and SnO_2/$CdSe_xTe_{1-x}$ devices across a range of processing conditions. A series of samples were fabricated by depositing CdTe onto CdS, SnO_2 and CdSe coated substrates at growth pressures between 5 – 400 Torr. These were then processed into devices following $MgCl_2$ treatment at temperatures between 410 – 430°C. The structure and morphology of the as grown films, as well as the performance of the complete solar cells, was compared directly across 84 processing conditions. The orientation of the CdTe films grown onto CdS show a strong dependence on growth conditions, becoming increasingly randomised at higher pressure. This was not observed for growth on SnO_2 or CdSe and therefore may imply that CdS is important in templating the subsequent growth of CdTe. Whilst SnO_2 offers a more transparent and robust substrate on which to grow CdTe devices, performance was hindered by poor growth at high pressure and a defective junction interface. Coating the SnO_2 substrate with a CdSe layer onto prior to CdTe deposition resulted in a more favourable growth surface, as well as an improved interface giving higher V_{oc} and fill factor in devices compared to direct growth onto SnO_2. Intermixing during the prolonged CdTe deposition onto CdSe also produces an intermixed $CdSe_xTe_{1-x}$ phase, which lowers the band gap and therefore improves infrared collection. However, since the intermixing and therefore the selenium profile throughout the absorber layer is dependent upon the CdTe growth and $MgCl_2$ activation conditions, it is difficult to isolate the effect this has on device performance from changes, for example on the grain structure and junction formation, which occur in parallel.

8.2 Suggestions for future work

8.2.1 Organic contacts for CdTe solar cells

Three commonly used organic compounds were investigated as potential contact layers for CdTe solar cells in this work, however the potential offered by organic chemistry is enormous and a vast array of possibilities remain. In theory, an ideal contact would possess a large valence band offset to act as an electron reflector, and a staggered conduction band offset between that of the CdTe valence band and metal work function in order to facilitate hole extraction. The wide parameter space allows fine tuning of organic semiconductors and therefore provides an ideal platform to test the effectiveness of such band offsets at the back contact. Systematically modifying a single organic semiconductor, as opposed to replacing the layer with an entirely different compound, could offer a more controllable route to determining the importance of the HOMO and LUMO levels whilst limiting the number of variables changed for each sample. Doping of the organic layer is also worth studying in further detail, especially in the case of PFO which lowered the back contact barrier height and effectively blocked pinholes, but limited performance due to its low conductivity and therefore additional series resistance. The dependence of the conductivity of the organic layer on its ability to prevent efficiency loss due to pinholes should also be explored further.

8.2.2 Alkali metals for doping and chlorine activation

The effect of sodium on the performance of CdTe solar cells is relatively unexplored in literature despite its likely presence as an unintentional impurity in most devices. The addition of NaF into the device stack has been shown to significantly impact performance, however the exact nature of its influence on the properties of the CdTe layer remains unclear. Differential scanning calorimetry measurements of compounds in the CdTe-$CdCl_2$-NaCl mixed phase system could provide a better understanding of the enhanced recrystallization induced by the presence of sodium in the chlorine activation and determine whether a lower temperature eutectic point exists. A combined Na and Cl treatment has been suggested for more effective grain boundary passivation in the literature, and indeed an improvement in device performance has been shown in this work. However, direct evidence of such a passivation effect has not been shown and therefore further study of the effect of sodium on grain boundaries in CdTe would be beneficial. Replacing the NaF as a source of sodium with NaCl or metallic Na would definitively exclude the influence of fluorine on device performance and lead to a simpler defect structure. Furthermore, the use of a higher quality substrate such as quartz or sapphire and/or a thicker sodium diffusion blocking layer, along

with high purity CdTe source material, would allow the effect of intentional sodium incorporation to be assessed in isolation from these unintentional impurities.

Whilst sodium has been focused on in this thesis, the heavier alkali metals also warrant further examination and their effect on CdTe is almost entirely unexplored in the literature. They offer the potential for improved *p*-type doping via substitutional incorporation onto Cd sites, and are likely to be less mobile in the CdTe lattice due to their larger atomic radius. The addition of NaF prior to the $MgCl_2$ activation treatment has been shown here to improve device efficiency for SnO_2/CdTe devices. The influence of other group I metals during the chlorine activation may be expected to have a similar effect as sodium and should also be considered. Heavier group I metals will have a larger ionic radius and would therefore be expected to be less mobile, and Rb in particular is likely to be better suited to occupying a vacant cadmium site with minimal lattice distortion.

8.2.3 Optimisation and characterisation of SnO_2/$CdSe_xTe_{1-x}$ device structure

The use of a selenium graded absorber layer partner with a wide band gap oxide window layer such as $Mg_xZn_{1-x}O$ or SnO_2 is rapidly becoming the standard device architecture for CdTe solar cells. This work has demonstrated that different growth substrates can strongly influence the resulting microstructure of CdTe layers, which can in turn impact device performance. Depositing CdTe layers directly onto SnO_2 was shown to produce poor quality, non-continuous films at high growth pressures. To understand this in more detail, the impact of the substrate on the nucleation and early stage growth of the CdTe overlayer should be studied further, whilst considering the effect of substrate roughness, surface chemistry and crystal structure. Although depositing a CdSe layer between the SnO_2 and CdTe improves the growth of the absorber layer, this relies on interdiffusion between the two layers and is prone to Kirkendall voiding. Deposition of a $CdSe_xTe_{1-x}$ layer directly onto SnO_2 may suffer from similarly poor growth as for CdTe, and therefore it is important to establish deposition conditions which ensure complete coverage of large grained, unstrained films.

Since samples were grown on SnO_2 layers coated by the manufacturer in the course of this work, it was not possible to study the influence of this layer in detail. Whilst commercially coated SnO_2 substrates offer a more convenient and reproducible growth surface, it does not afford any control over the processing conditions and therefore sample characteristics. Depositing the SnO_2 layer in-house would allow the effect of work function, resistivity, and morphology to be studied further. The band alignment between SnO_2 and CdTe should also be explored further. Photoemission measurements would be beneficial to compare the true band alignment to that predicted from literature values, and to the SnO_2/$CdSe_xTe_{1-x}$ interface.